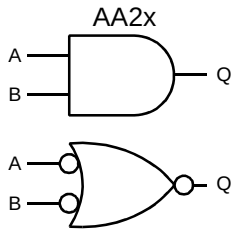
Description

AA2x is a family of 2-input gates which perform the logical AND function.

Logic Symbol



Truth Table

A	B	Q
L	L	L
L	H	L
H	L	L
H	H	H

HDL Syntax

Verilog ..... AA2x *inst_name* (Q, A, B);

VHDL..... *inst_name*: AA2x port map (Q, A, B);

Pin Loading

Pin Name	Equivalent Loads			
	AA21	AA22	AA24	AA26
A	1.0	1.0	2.1	2.1
B	1.0	1.0	2.1	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AA21	2.0	TBD	2.8
AA22	2.0	TBD	3.9
AA24	4.0	TBD	7.0
AA26	5.0	TBD	10.5

a. See page 2-15 for power equation.

AMI5HG 0.5 micron CMOS Gate Array

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

AA21	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.27 0.22	0.36 0.33	0.49 0.46	0.64 0.61	0.76 0.72
AA22	**Number of Equivalent Loads**		**1**	**8**	**15**	**22**	**30 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.31 0.26	0.43 0.39	0.53 0.48	0.63 0.57	0.75 0.69
AA24	**Number of Equivalent Loads**		**1**	**14**	**28**	**42**	**56 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.30 0.21	0.41 0.33	0.49 0.44	0.57 0.54	0.64 0.65
AA26	**Number of Equivalent Loads**		**1**	**21**	**42**	**62**	**83 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.34 0.26	0.47 0.39	0.55 0.50	0.64 0.60	0.74 0.70

Delay will vary with input conditions. See page 2-17 for interconnect estimates.