Stack Module Features

- 64-Mbit Flash + 16-Mbit PSRAM
- Power Supply of 2.7V to 3.1V
- Data I/O x16
- 66-ball CBGA Package: 8 x 11x 1.0 mm

64-Mbit Flash Features

- 64-megabit (4M x 16) Flash Memory
- 2.7V - 3.1V Read/Write
- High Performance
  - Asynchronous Access Time – 70, 85 ns
- Sector Erase Architecture
  - Eight 4K Word Sectors with Individual Write Lockout
  - 32K Word Main Sectors with Individual Write Lockout
- Typical Sector Erase Time: 32K Word Sectors – 500 ms; 4K Word Sectors – 100 ms
- 64M, Four Plane Organization, Permitting Concurrent Read in Any of Three Planes not Being Programmed/Erased
  - Memory Plane A: 16M of Memory Including Eight 4K Word Sectors
  - Memory Plane B: 16M of Memory Consisting of 32K Word Sectors
  - Memory Plane C: 16M of Memory Consisting of 32K Word Sectors
  - Memory Plane D: 16M of Memory Consisting of 32K Word Sectors
- Suspend/Resume Feature for Erase and Program
  - Supports Reading and Programming Data from Any Sector by Suspending Erase of a Different Sector
  - Supports Reading Any Word by Suspending Programming of Any Other Word
- Low-power Operation
  - 30 mA Active
  - 35 µA Standby
- 1.8V I/O Option Reduces Overall System Power
- $\overline{\text{Data}}$ Polling and Toggle Bit for End of Program Detection
- VPP Pin for Write Protection and Accelerated Program/Erase Operations
- $\overline{\text{RESET}}$ Input for Device Initialization
- Top or Bottom Boot Block Configuration Available
- 128-bit Protection Register
- Common Flash Interface (CFI)

16-Mbit PSRAM Features

- 16-Mbit (1M x 16)
- 2.7V to 3.1V V_{CC} Operation
- 70 ns Access Time

Stack Module Description

The AT52BC6402A(T) consists of a 64-Mbit Flash stacked with a 16-Mbit PSRAM in a single CBGA package.

Stack Module Memory Contents

Device	Memory Combination	Flash/PSRAM Read Access
AT52BC6402A(T)	64M Flash + 16M PSRAM	Asynchronous, Page Mode

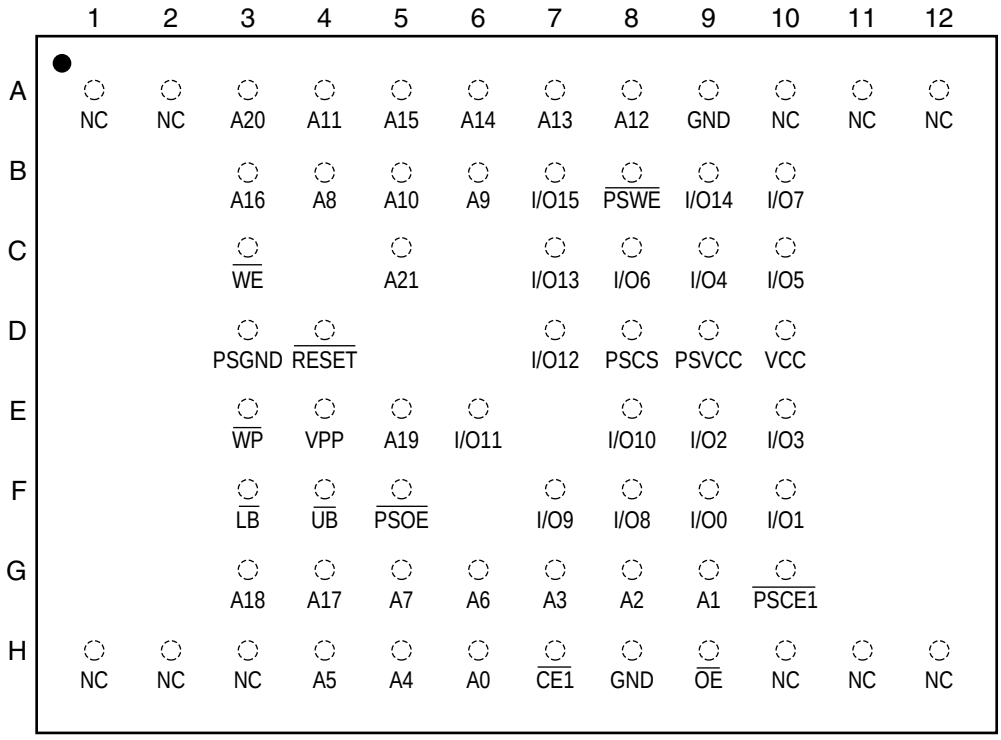
64-Mbit Flash, 16-Mbit PSRAM (x16 I/O)

AT52BC6402A
AT52BC6402AT

Preliminary

Rev. 3441B–STKD–11/04

66C4 – CBGA
Top View



Pin Configurations

Pin Name	Function
A0 - A21	Address
I/O0 - I/O15	Data Inputs/Outputs
$\overline{CE1}$	Flash Chip Enable
$\overline{PSCE1}$	PSRAM Chip Enable
PSCS	PSRAM Chip Select (Deep Power-down Control – Mode Pin)
$\overline{OE}$/$\overline{PSOE}$	Flash Output Enable/PSRAM Output Enable
$\overline{WE}$/$\overline{PSWE}$	Flash Write Enable/PSRAM Write Enable
$\overline{LB}$	Lower Byte Control (PSRAM)
$\overline{UB}$	Upper Byte Control (PSRAM)
$\overline{RESET}$	Flash Reset
$\overline{WP}$	Flash Write Protect
VPP	Flash Write Protection and Power Supply for Accelerated Program/Erase Operation
VCC/PSVCC	Flash Power Supply/PSRAM Power Supply
NC	No Connect
GND/PSGND	Device Ground/PSRAM Ground

64-Mbit Flash Description

The 64-Mbit Flash memory is divided into multiple sectors and planes for erase operations. The devices can be read or reprogrammed off a single 2.7V power supply, making them ideally suited for in-system programming.

The 64-Mbit device is divided into four memory planes. A read operation can occur in any of the three planes which is not being programmed or erased. This concurrent operation allows improved system performance by not requiring the system to wait for a program or erase operation to complete before a read is performed. To further increase the flexibility of the device, it contains an Erase Suspend and Program Suspend feature. This feature will put the erase or program on hold for any amount of time and let the user read data from or program data to any of the remaining sectors. There is no reason to suspend the erase or program operation if the data to be read is in another memory plane. The end of program or erase is detected by $\overline{\text{Data}}$ Polling or toggle bit.

The VPP pin provides data protection and faster programming and erase times. When the V_{PP} input is below 0.8V, the program and erase functions are inhibited. When V_{PP} is at 1.65V or above, normal program and erase operations can be performed. With V_{PP} at 12.0V, the program and erase operations are accelerated.

With V_{PP} at 12V, a six-byte command (Enter Single Pulse Program Mode) to remove the requirement of entering the three-byte program sequence is offered to further improve programming time. After entering the six-byte code, only single pulses on the write control lines are required for writing into the device. This mode (Single Pulse Word Program) is exited by powering down the device, by taking the $\overline{\text{RESET}}$ pin to GND or by a high-to-low transition on the V_{PP} input. Erase, Erase Suspend/Resume, Program Suspend/Resume and Read Reset commands will not work while in this mode; if entered they will result in data being programmed into the device. It is not recommended that the six-byte code reside in the software of the final product but only exist in external programming code.

Device Operation

COMMAND SEQUENCES: The device powers on in the read mode. Command sequences are used to place the device in other operating modes such as program and erase. After the completion of a program or an erase cycle, the device enters the read mode. The command sequences are written by applying a low pulse on the $\overline{\text{WE}}$ input with $\overline{\text{CE}}$ low and $\overline{\text{OE}}$ high or by applying a low-going pulse on the $\overline{\text{CE}}$ input with $\overline{\text{WE}}$ low and $\overline{\text{OE}}$ high. The address is latched on the falling edge of the $\overline{\text{WE}}$ or $\overline{\text{CE}}$ pulse whichever occurs first. Valid data is latched on the rising edge of the $\overline{\text{WE}}$ or the $\overline{\text{CE}}$ pulse, whichever occurs first. The addresses used in the command sequences are not affected by entering the command sequences.

ASYNCHRONOUS READ: The 64-Mbit Flash is accessed like an EPROM. When $\overline{\text{CE}}$ and $\overline{\text{OE}}$ are low and $\overline{\text{WE}}$ is high, the data stored at the memory location determined by the address pins are asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{\text{CE}}$ or $\overline{\text{OE}}$ is high. This dual-line control gives designers flexibility in preventing bus contention.

RESET: A $\overline{\text{RESET}}$ input pin is provided to ease some system applications. When $\overline{\text{RESET}}$ is at a logic high level, the device is in its standard operating mode. A low level on the $\overline{\text{RESET}}$ pin halts the present device operation and puts the outputs of the device in a high-impedance state. When a high level is reasserted on the $\overline{\text{RESET}}$ pin, the device returns to read or standby mode, depending upon the state of the control pins.

ERASE: Before a word can be reprogrammed it must be erased. The erased state of the memory bits is a logical “1”. The entire memory can be erased by using the Chip Erase command or individual planes or sectors can be erased by using the Plane Erase or Sector Erase commands.

CHIP ERASE: Chip Erase is a six-bus cycle operation. The automatic erase begins on the rising edge of the last $\overline{WE}$ pulse. Chip Erase does not alter the data of the protected sectors. After the full chip erase the device will return back to the read mode. The hardware reset during Chip Erase will stop the erase but the data will be of unknown state. Any command during Chip Erase except Erase Suspend will be ignored.

PLANE ERASE: As a alternative to a full chip erase, the device is organized into four planes that can be individually erased. The plane erase command is a six-bus cycle operation. The plane whose address is valid at the sixth falling edge of $\overline{WE}$ will be erased provided none of the sectors within the plane are protected.

SECTOR ERASE: As an alternative to a full chip erase or a plane erase, the device is organized into multiple sectors that can be individually erased. The Sector Erase command is a six-bus cycle operation. The sector whose address is valid at the sixth falling edge of $\overline{WE}$ will be erased provided the given sector has not been protected.

WORD PROGRAMMING: The device is programmed on a word-by-word basis. Programming is accomplished via the internal device command register and is a four-bus cycle operation. The programming address and data are latched in the fourth cycle. The device will automatically generate the required internal programming pulses. Please note that a “0” cannot be programmed back to a “1”; only erase operations can convert “0”s to “1”s.

FLEXIBLE SECTOR PROTECTION: The 64-Mbit device offers two sector protection modes, the Softlock and the Hardlock. The Softlock mode is optimized as sector protection for sectors whose content changes frequently. The Hardlock protection mode is recommended for sectors whose content changes infrequently. Once either of these two modes is enabled, the contents of the selected sector is read-only and cannot be erased or programmed. Each sector can be independently programmed for either the Softlock or Hardlock sector protection mode. At power-up and reset, all sectors have their Softlock protection mode enabled.

SOFTLOCK AND UNLOCK: The Softlock protection mode can be disabled by issuing a two-bus cycle Unlock command to the selected sector. Once a sector is unlocked, its contents can be erased or programmed. To enable the Softlock protection mode, a six-bus cycle Softlock command must be issued to the selected sector.

HARDLOCK AND WRITE PROTECT ($\overline{WP}$): The Hardlock sector protection mode operates in conjunction with the Write Protection ($\overline{WP}$) pin. The Hardlock sector protection mode can be enabled by issuing a six-bus cycle Hardlock software command to the selected sector. The state of the Write Protect pin affects whether the Hardlock protection mode can be overridden.

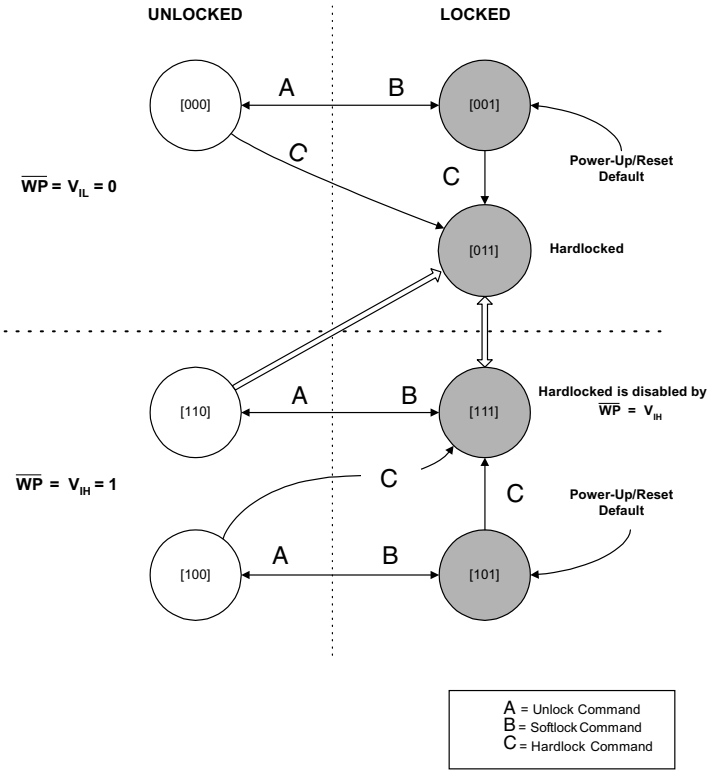
- When the $\overline{WP}$ pin is low and the Hardlock protection mode is enabled, the sector cannot be unlocked and the contents of the sector is read-only.
- When the $\overline{WP}$ pin is high, the Hardlock protection mode is overridden and the sector can be unlocked via the Unlock command.

To disable the Hardlock sector protection mode, the chip must be either reset or power cycled.

Table 1. Hardlock and Softlock Protection Configurations in Conjunction with $\overline{WP}$

V_{PP}	$\overline{WP}$	Hard-lock	Soft-lock	Erase/ Prog Allowed?	Comments
V_{CC}/5V	0	0	0	Yes	No sector is locked
V_{CC}/5V	0	0	1	No	Sector is Softlocked. The Unlock command can unlock the sector.
V_{CC}/5V	0	1	1	No	Hardlock protection mode is enabled. The sector cannot be unlocked.
V_{CC}/5V	1	0	0	Yes	No sector is locked.
V_{CC}/5V	1	0	1	No	Sector is Softlocked. The Unlock command can unlock the sector.
V_{CC}/5V	1	1	0	Yes	Hardlock protection mode is overridden and the sector is not locked.
V_{CC}/5V	1	1	1	No	Hardlock protection mode is overridden and the sector can be unlocked via the Unlock command.
V_{IL}	x	x	x	No	Erase and Program Operations cannot be performed.

Figure 1. Sector Locking State Diagram



Note: 1. The notation [X, Y, Z] denotes the locking state of a sector. The current locking state of a sector is defined by the state of $\overline{WP}$ and the two bits of the sector-lock status D[1:0].

SECTOR PROTECTION DETECTION: A software method is available to determine if the sector protection Softlock or Hardlock features are enabled. When the device is in the software product identification mode (see Software Product Identification Entry and Exit sections) a read from the I/O0 and I/O1 at address location 00002H within a sector will show if the sector is unlocked, softlocked, or hardlocked.

Table 2. Sector Protection Status

I/O1	I/O0	Sector Protection Status
0	0	Sector Not Locked
0	1	Softlock Enabled
1	0	Hardlock Enabled
1	1	Both Hardlock and Softlock Enabled

PROGRAM/ERASE STATUS: The device provides several bits to determine the status of a program or erase operation: I/O2, I/O3, I/O5, I/O6, and I/O7. All other status bits are don't care. Table 3 on page 11 and the following four sections describe the function of these bits. To provide greater flexibility for system designers, the 64-Mbit device contains a programmable configuration register. The configuration register allows the user to specify the status bit operation. The configuration register can be set to one of two different values, "00" or "01". If the configuration register is set to "00", the part will automatically return to the read mode after a successful program or erase operation. If the configuration register is set to a "01", a Product ID Exit command must be given after a successful program or erase operation before the part will return to the read mode. It is important to note that whether the configuration register is set to a "00" or to a "01", any unsuccessful program or erase operation requires using the Product ID Exit command to return the device to read mode. The default value (after power-up) for the configuration register is "00". Using the four-bus cycle set configuration register command as shown in the Command Definition table on page 12, the value of the configuration register can be changed. Voltages applied to the reset pin will not alter the value of the configuration register. The value of the configuration register will affect the operation of the I/O7 status bit as described below.

$\overline{\text{DATA}}$ POLLING: The 64-Mbit device features $\overline{\text{Data}}$ Polling to indicate the end of a program cycle. If the status configuration register is set to a "00", during a program cycle an attempted read of the last word loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. During a chip or sector erase operation, an attempt to read the device will give a "0" on I/O7. Once the program or erase cycle has completed, true data will be read from the device. $\overline{\text{Data}}$ Polling may begin at any time during the program cycle. Please see Table 3 on page 11 for more details.

If the status bit configuration register is set to a "01", the I/O7 status bit will be low while the device is actively programming or erasing data. I/O7 will go high when the device has completed a program or erase operation. Once I/O7 has gone high, status information on the other pins can be checked.

The $\overline{\text{Data}}$ Polling status bit must be used in conjunction with the erase/program and V_{PP} status bit as shown in the algorithm in Figures 2 and 3.

TOGGLE BIT: In addition to $\overline{\text{Data}}$ Polling, the 64-Mbit device provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the memory will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling

and valid data will be read. Examining the toggle bit may begin at any time during a program cycle. Please see Table 3 on page 11 for more details.

The toggle bit status bit should be used in conjunction with the erase/program and V_{PP} status bit as shown in the algorithm in Figures 4 and 5 on page 10.

ERASE/PROGRAM STATUS BIT: The device offers a status bit on I/O5 that indicates whether the program or erase operation has exceeded a specified internal pulse count limit. If the status bit is a “1”, the device is unable to verify that an erase or a word program operation has been successfully performed. The device may also output a “1” on I/O5 if the system tries to program a “1” to a location that was previously programmed to a “0”. Only an erase operation can change a “0” back to a “1”. If a program (Sector Erase) command is issued to a protected sector, the protected sector will not be programmed (erased). The device will go to a status read mode and the I/O5 status bit will be set high, indicating the program (erase) operation did not complete as requested. Once the erase/program status bit has been set to a “1”, the system must write the Product ID Exit command to return to the read mode. The erase/program status bit is a “0” while the erase or program operation is still in progress. Please see Table 3 on page 11 for more details.

V_{PP} STATUS BIT: The 64-Mbit device provides a status bit on I/O3 that provides information regarding the voltage level of the VPP pin. During a program or erase operation, if the voltage on the VPP pin is not high enough to perform the desired operation successfully, the I/O3 status bit will be a “1”. Once the V_{PP} status bit has been set to a “1”, the system must write the Product ID Exit command to return to the read mode. On the other hand, if the voltage level is high enough to perform a program or erase operation successfully, the V_{PP} status bit will output a “0”. Please see Table 3 on page 11 for more details.

ERASE SUSPEND/ERASE RESUME: The Erase Suspend command allows the system to interrupt a sector erase operation and then program or read data from a different sector within the same plane. Since this device has a multiple plane architecture, there is no need to use the erase suspend feature while erasing a sector when you want to read data from a sector in another plane. After the Erase Suspend command is given, the device requires a maximum time of 15 µs to suspend the erase operation. After the erase operation has been suspended, the plane that contains the suspended sector enters the erase-suspend-read mode. The system can then read data or program data to any other sector within the device. An address is not required during the Erase Suspend command. During a sector erase suspend, another sector cannot be erased. To resume the sector erase operation, the system must write the Erase Resume command. The Erase Resume command is a one-bus cycle command, which does require the plane address. The device also supports an erase suspend during a complete chip erase. While the chip erase is suspended, the user can read from any sector within the memory that is protected. The command sequence for a chip erase suspend and a sector erase suspend are the same.

PROGRAM SUSPEND/PROGRAM RESUME: The Program Suspend command allows the system to interrupt a programming operation and then read data from a different word within the memory. After the Program Suspend command is given, the device requires a maximum of 10 µs to suspend the programming operation. After the programming operation has been suspended, the system can then read from any other word within the device. An address is not required during the program suspend operation. To resume the programming operation, the system must write the Program Resume command. The program suspend and resume are one-bus cycle commands. The command sequence for the erase suspend and program suspend are the same, and the command sequence for the erase resume and program resume are the same.

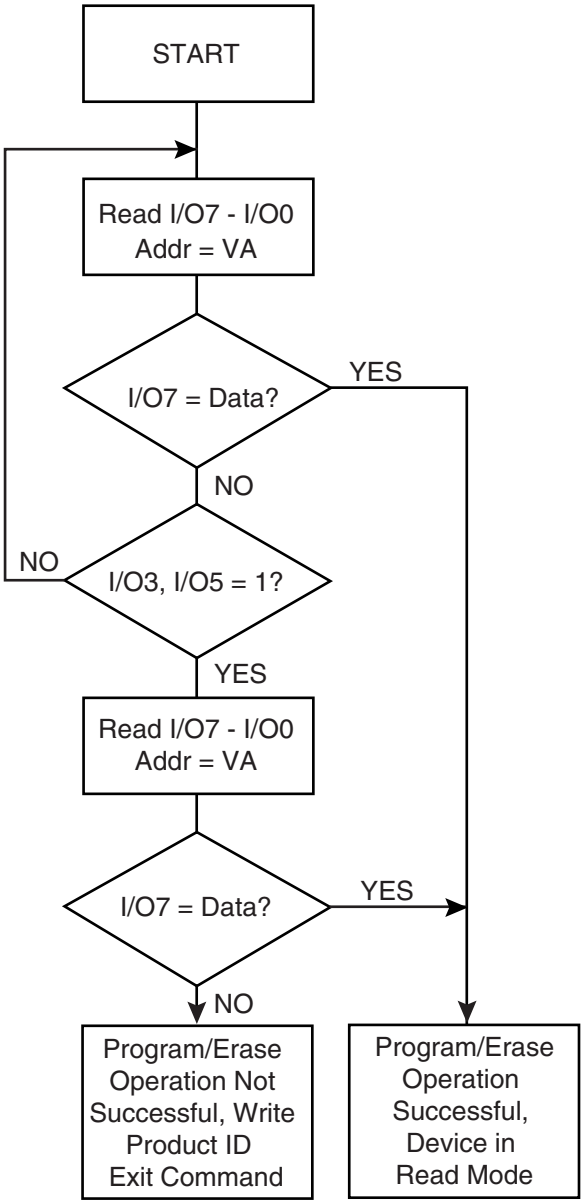
128-BIT PROTECTION REGISTER: The 64-Mbit device contains a 128-bit register that can be used for security purposes in system design. The protection register is divided into two 64-bit blocks. The two blocks are designated as block A and block B. The data in block A is non-changeable and is programmed at the factory with a unique number. The data in block B is programmed by the user and can be locked out such that data in the block cannot be reprogrammed. To program block B in the protection register, the four-bus cycle Program Protection Register command must be used as shown in the Command Definition table on page 12. To lock out block B, the four-bus cycle lock protection register command must be used as shown in the Command Definition table. Data bit D1 must be zero during the fourth bus cycle. All other data bits during the fourth bus cycle are don't cares. To determine whether block B is locked out, the status of Block B Protection command is given. If data bit D1 is zero, block B is locked. If data bit D1 is one, block B can be reprogrammed. Please see the Protection Register Addressing Table on page 13 for the address locations in the protection register. To read the protection register, the Product ID Entry command is given followed by a normal read operation from an address within the protection register. After determining whether block B is protected or not or reading the protection register, the Product ID Exit command must be given prior to performing any other operation.

CFI: Common Flash Interface (CFI) is a published, standardized data structure that may be read from a Flash device. CFI allows system software to query the installed device to determine the configurations, various electrical and timing parameters, and functions supported by the device. CFI is used to allow the system to learn how to interface to the Flash device most optimally. The two primary benefits of using CFI are ease of upgrading and second source availability. The command to enter the CFI Query mode is a one-bus cycle command which requires writing data 98h to address 55h. The CFI Query command can be written when the device is ready to read data or can also be written when the part is in the product ID mode. Once in the CFI Query mode, the system can read CFI data at the addresses given in Table 4 on page 24. To exit the CFI Query mode, the product ID exit command must be given. If the CFI Query command is given while the part is in the product ID mode, then the product ID exit command must first be given to return the part to the product ID mode. Once in the product ID mode, it will be necessary to give another product ID exit command to return the part to the read mode.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the 64-Mbit device in the following ways: (a) V_{CC} sense: if V_{CC} is below 1.8V (typical), the program function is inhibited. (b) V_{CC} power-on delay: once V_{CC} has reached the V_{CC} sense level, the device will automatically time-out 10 ms (typical) before programming. (c) Program inhibit: holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles. (d) Noise filter: pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle. (e) V_{PP} is less than V_{ILPP}.

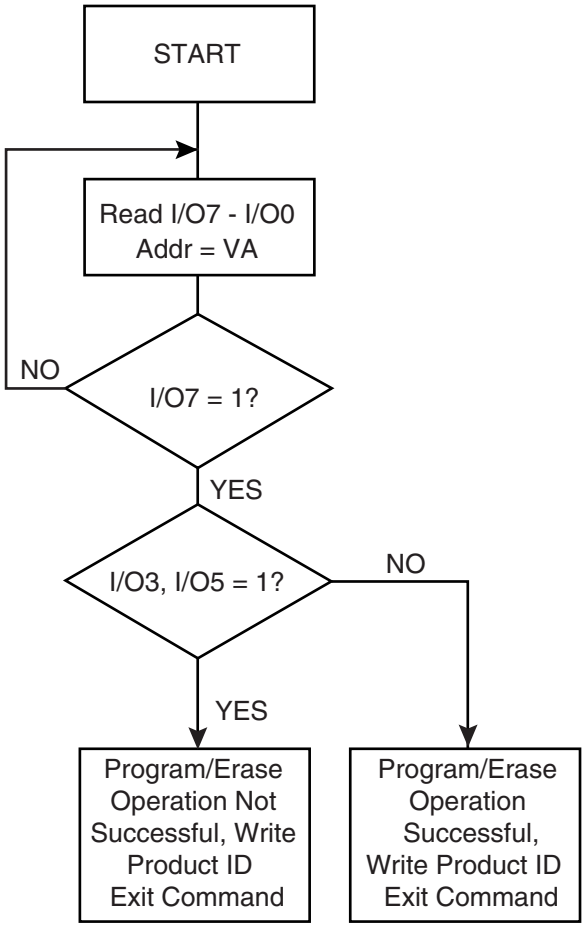
INPUT LEVELS: While operating with a 2.7V to 3.1V power supply, the address inputs and control inputs ($\overline{OE}$, $\overline{CE}$ and $\overline{WE}$) may be driven from 0 to 5.5V without adversely affecting the operation of the device. The I/O lines can be driven from 0 to V_{CCQ} + 0.6V.

Figure 2. $\overline{\text{Data}}$ Polling Algorithm
(Configuration Register = 00)



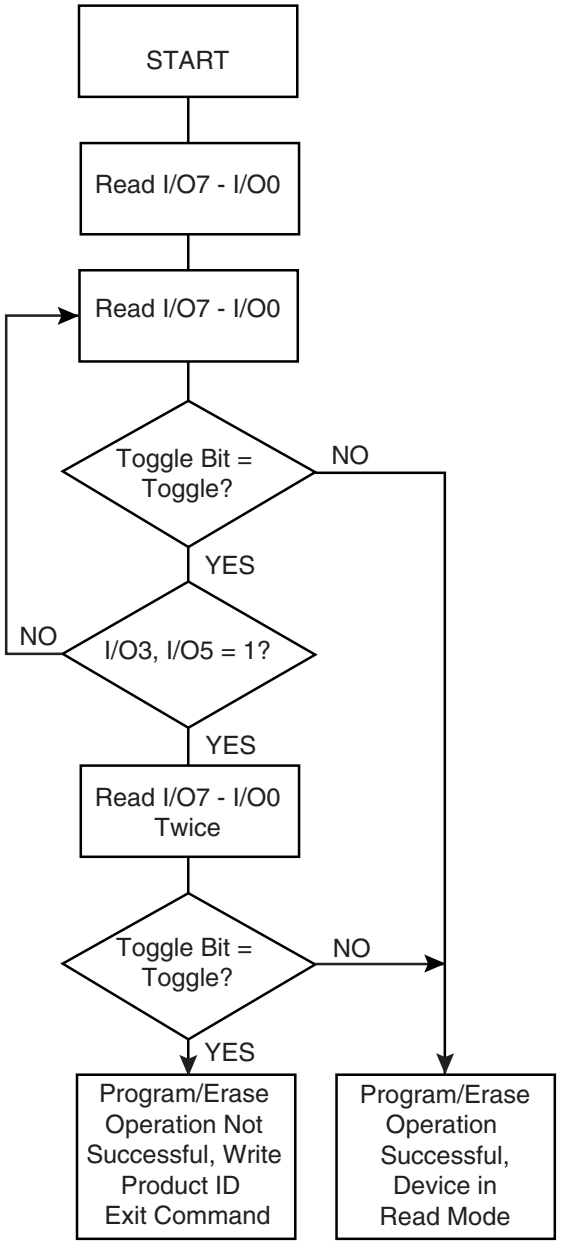
Notes: 1. VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.
2. I/O7 should be rechecked even if I/O5 = "1" because I/O7 may change simultaneously with I/O5.

Figure 3. $\overline{\text{Data}}$ Polling Algorithm
(Configuration Register = 01)



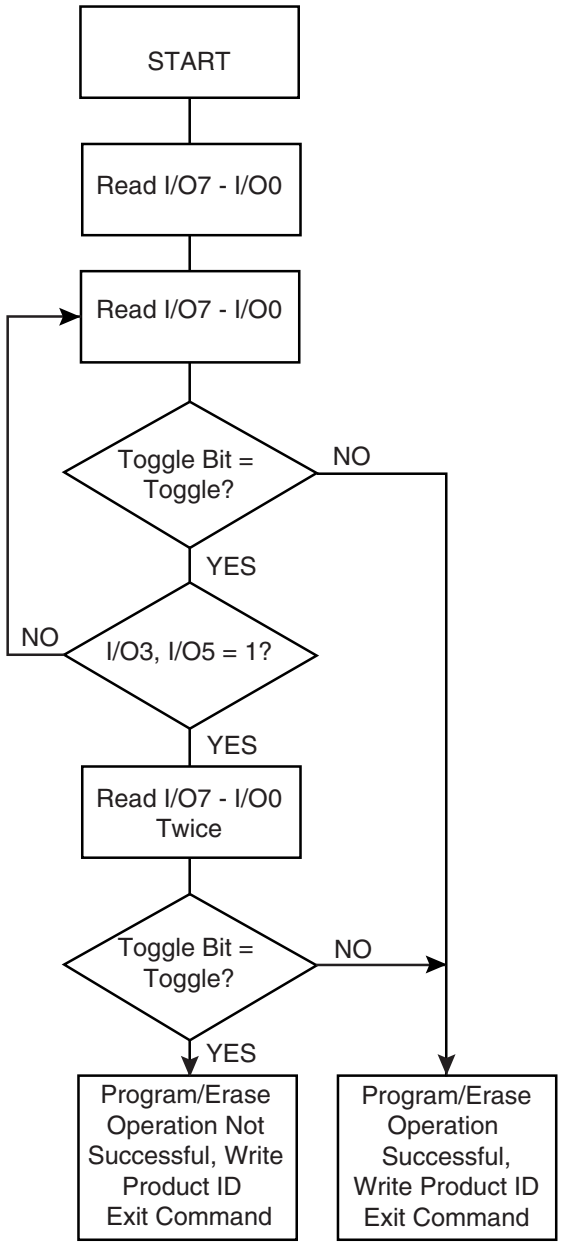
Note: 1. VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.

Figure 4. Toggle Bit Algorithm (Configuration Register = 00)



Note: 1. The system should recheck the toggle bit even if I/O5 = “1” because the toggle bit may stop toggling as I/O5 changes to “1”.

Figure 5. Toggle Bit Algorithm (Configuration Register = 01)



Note: 1. The system should recheck the toggle bit even if I/O5 = “1” because the toggle bit may stop toggling as I/O5 changes to “1”.

Table 3. Status Bit Table

	I/O7				I/O6				I/O2			
Configuration Register:	**00/01**	**00/01**	**00/01**	**00/01**	**00/01**	**00/01**	**00/01**	**00/01**	**00/01**	**00/01**	**00/01**	**00/01**
Read Address In	Plane A	Plane B	Plane C	Plane D	Plane A	Plane B	Plane C	Plane D	Plane A	Plane B	Plane C	Plane D
While												
Programming in Plane A	$\overline{I/O7}$/0	DATA	DATA	DATA	TOGGLE	DATA	DATA	DATA	1	DATA	DATA	DATA
Programming in Plane B	DATA	$\overline{I/O7}$/0	DATA	DATA	DATA	TOGGLE	DATA	DATA	DATA	1	DATA	DATA
Programming in Plane C	DATA	DATA	$\overline{I/O7}$/0	DATA	DATA	DATA	TOGGLE	DATA	DATA	DATA	1	DATA
Programming in Plane D	DATA	DATA	DATA	$\overline{I/O7}$/0	DATA	DATA	DATA	TOGGLE	DATA	DATA	DATA	1
Erasing in Plane A	0/0	DATA	DATA	DATA	TOGGLE	DATA	DATA	DATA	TOGGLE	DATA	DATA	DATA
Erasing in Plane B	DATA	0/0	DATA	DATA	DATA	TOGGLE	DATA	DATA	DATA	TOGGLE	DATA	DATA
Erasing in Plane C	DATA	DATA	0/0	DATA	DATA	DATA	TOGGLE	DATA	DATA	DATA	TOGGLE	DATA
Erasing in Plane D	DATA	DATA	DATA	0/0	DATA	DATA	DATA	TOGGLE	DATA	DATA	DATA	TOGGLE
Erase Suspended & Read Erasing Sector	1	1	1	1	1	1	1	1	TOGGLE	TOGGLE	TOGGLE	TOGGLE
Erase Suspended & Read Non-erasing Sector	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
Erase Suspended & Program Non-erasing Sector in Plane A	$\overline{I/O7}$/0	DATA	DATA	DATA	TOGGLE	DATA	DATA	DATA	TOGGLE	DATA	DATA	DATA
Erase Suspended & Program Non-erasing Sector in Plane B	DATA	$\overline{I/O7}$/0	DATA	DATA	DATA	TOGGLE	DATA	DATA	DATA	TOGGLE	DATA	DATA
Erase Suspended & Program Non-erasing Sector in Plane C	DATA	DATA	$\overline{I/O7}$/0	DATA	DATA	DATA	TOGGLE	DATA	DATA	DATA	TOGGLE	DATA
Erase Suspended & Program Non-erasing Sector in Plane D	DATA	DATA	DATA	$\overline{I/O7}$/0	DATA	DATA	DATA	TOGGLE	DATA	DATA	DATA	TOGGLE

Command Definition (Hex)[1]

Command Sequence	Bus Cycles	1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle		4th Bus Cycle		5th Bus Cycle		6th Bus Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read	1	Addr	D_{OUT}										
Chip Erase	6	555	AA	AAA[2]	55	555	80	555	AA	AAA	55	555	10
Plane Erase	6	555	AA	AAA	55	555	80	555	AA	AAA	55	PA[6]	20
Sector Erase	6	555	AA	AAA	55	555	80	555	AA	AAA	55	SA[4]	30
Word Program	4	555	AA	AAA	55	555	A0	Addr	D_{IN}				
Dual-Word Program[8]	5	555	AA	AAA	55	555	A1	Addr0	D_{IN0}	Addr1	D_{IN1}		
Enter Single-pulse Program Mode	6	555	AA	AAA	55	555	80	555	AA	AAA	55	555	A0
Single-pulse Word Program Mode	1	Addr	D_{IN}										
Sector Softlock	6	555	AA	AAA	55	555	80	555	AA	AAA	55	SA[4]	40
Sector Unlock	2	555	AA	SA[4]	70								
Sector Hardlock	6	555	AA	AAA	55	555	80	555	AA	AAA	55	SA[4][5]	60
Erase/Program Suspend	1	xxx	B0										
Erase/Program Resume	1	PA[6]	30										
Product ID Entry[7]	3	555	AA	AAA	55	PA+00555	90						
Product ID Exit[3]	3	555	AA	AAA	55	555	F0						
Product ID Exit[3]	1	xxx	FX										
Program Protection Register – Block B	4	555	AA	AAA	55	555	C0	xxxx[12]8x[11]	D_{IN}				
Lock Protection Register – Block B	4	555	AA	AAA	55	555	C0	xxxx80[12]	X0				
Status of Block B Protection	4	555	AA	AAA	55	555	90	xxxx80[13]	D_{OUT}[9]				
Set Configuration Register	4	555	AA	AAA	55	555	E0	xxx	00/01[10]				
CFI Query	1	X55	98										

Notes:
1. The DATA FORMAT in each bus cycle is as follows: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex). The ADDRESS FORMAT in each bus cycle is as follows: A11 - A0 (Hex), A11 - A21 (Don't Care).
2. Since A11 is a Don't Care, AAA can be replaced with 2AA.
3. Either one of the Product ID Exit commands can be used.
4. SA = sector address. Any word address within a sector can be used to designate the sector address (see pages 14 - 17 for details).
5. Once a sector is in the Hardlock protection mode, it cannot be disabled unless the chip is reset or power cycled.
6. PA is the plane address (A21 - A20).
7. During the fourth bus cycle, the manufacturer code is read from address PA+00000H, the device code is read from address PA+00001H, and the data in the protection register is read from addresses 000081H - 000088H. PA (A21 - A20) must specify the same plane address as specified in the third bus cycle.
8. The fast programming option enables the user to program two words in parallel only when V_{PP} = 12V. The addresses, Addr0 and Addr1, of the two words, D_{IN0} and D_{IN1}, must only differ in address A0. This command should be used for manufacturing purpose only.
9. If data bit D1 is "0", block B is locked. If data bit D1 is "1", block B can be reprogrammed.
10. The default state (after power-up) of the configuration register is "00".
11. Any address within the user programmable register region. Please see "Protection Register Addressing Table" on page 13.
12. For the AT49BV6416, xxxx = 0000H. For the AT49BV6416T, xxxx = 3F80H.
13. For the AT49BV6416, xxxx = 0000H. For the AT49BV6416T, xxxx = 0F80H.

Absolute Maximum Ratings*

Temperature under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages Except V_{PP} (including NC Pins) with Respect to Ground	-0.6V to +6.25V
V_{PP} Input Voltage with Respect to Ground	0V to 13.0V
All Output Voltages with Respect to Ground	-0.6V to V_{CCQ} + 0.6V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Protection Register Addressing Table

Word	Use	Block	A7	A6	A5	A4	A3	A2	A1	A0
0	Factory	A	1	0	0	0	0	0	0	1
1	Factory	A	1	0	0	0	0	0	1	0
2	Factory	A	1	0	0	0	0	0	1	1
3	Factory	A	1	0	0	0	0	1	0	0
4	User	B	1	0	0	0	0	1	0	1
5	User	B	1	0	0	0	0	1	1	0
6	User	B	1	0	0	0	0	1	1	1
7	User	B	1	0	0	0	1	0	0	0

Memory Organization – 64-Mbit Bottom Boot

Plane	Sector	Size (Words)	x16 Address Range (A21 - A0)
A	SA0	4K	00000 - 00FFF
A	SA1	4K	01000 - 01FFF
A	SA2	4K	02000 - 02FFF
A	SA3	4K	03000 - 03FFF
A	SA4	4K	04000 - 04FFF
A	SA5	4K	05000 - 05FFF
A	SA6	4K	06000 - 06FFF
A	SA7	4K	07000 - 07FFF
A	SA8	32K	08000 - 0FFFF
A	SA9	32K	10000 - 17FFF
A	SA10	32K	18000 - 1FFFF
A	SA11	32K	20000 - 27FFF
A	SA12	32K	28000 - 2FFFF
A	SA13	32K	30000 - 37FFF
A	SA14	32K	38000 - 3FFFF
A	SA15	32K	40000 - 47FFF
A	SA16	32K	48000 - 4FFFF
A	SA17	32K	50000 - 57FFF
A	SA18	32K	58000 - 5FFFF
A	SA19	32K	60000 - 67FFF
A	SA20	32K	68000 - 6FFFF
A	SA21	32K	70000 - 77FFF
A	SA22	32K	78000 - 7FFFF
A	SA23	32K	80000 - 87FFF
A	SA24	32K	88000 - 8FFFF
A	SA25	32K	90000 - 97FFF
A	SA26	32K	98000 - 9FFFF
A	SA27	32K	A0000 - A7FFF
A	SA28	32K	A8000 - AFFFF
A	SA29	32K	B0000 - B7FFF
A	SA30	32K	B8000 - BFFFF
A	SA31	32K	C0000 - C7FFF
A	SA32	32K	C8000 - CFFFF
A	SA33	32K	D0000 - D7FFF
A	SA34	32K	D8000 - DFFFF
A	SA35	32K	E0000 - E7FFF
A	SA36	32K	E8000 - EFFFF
A	SA37	32K	F0000 - F7FFF
A	SA38	32K	F8000 - FFFFF
B	SA39	32K	100000 - 107FFF
B	SA40	32K	108000 - 10FFFF
B	SA41	32K	110000 - 117FFF
B	SA42	32K	118000 - 11FFFF
B	SA43	32K	120000 - 127FFF
B	SA44	32K	128000 - 12FFFF

Memory Organization – 64-Mbit Bottom Boot (Continued)

Plane	Sector	Size (Words)	x16 Address Range (A21 - A0)
B	SA45	32K	130000 - 137FFF
B	SA46	32K	138000 - 13FFFF
B	SA47	32K	140000 - 147FFF
B	SA48	32K	148000 - 14FFFF
B	SA49	32K	150000 - 157FFF
B	SA50	32K	158000 - 15FFFF
B	SA51	32K	160000 - 167FFF
B	SA52	32K	168000 - 16FFFF
B	SA53	32K	170000 - 177FFF
B	SA54	32K	178000 - 17FFFF
B	SA55	32K	180000 - 187FFF
B	SA56	32K	188000 - 18FFFF
B	SA57	32K	190000 - 197FFF
B	SA58	32K	198000 - 19FFFF
B	SA59	32K	1A0000 - 1A7FFF
B	SA60	32K	1A8000 - 1AFFFF
B	SA61	32K	1B0000 - 1B7FFF
B	SA62	32K	1B8000 - 1BFFFF
B	SA63	32K	1C0000 - 1C7FFF
B	SA64	32K	1C8000 - 1CFFFF
B	SA65	32K	1D0000 - 1D7FFF
B	SA66	32K	1D8000 - 1DFFFF
B	SA67	32K	1E0000 - 1E7FFF
B	SA68	32K	1E8000 - 1EFFFF
B	SA69	32K	1F0000 - 1F7FFF
B	SA70	32K	1F8000 - 1FFFFF
C	SA71	32K	200000 - 207FFF
C	SA72	32K	208000 - 20FFFF
C	SA73	32K	210000 - 217FFF
C	SA74	32K	218000 - 21FFFF
C	SA75	32K	220000 - 227FFF
C	SA76	32K	228000 - 22FFFF
C	SA77	32K	230000 - 237FFF
C	SA78	32K	238000 - 23FFFF
C	SA79	32K	240000 - 247FFF
C	SA80	32K	248000 - 24FFFF
C	SA81	32K	250000 - 257FFF
C	SA82	32K	258000 - 25FFFF
C	SA83	32K	260000 - 267FFF
C	SA84	32K	268000 - 26FFFF
C	SA85	32K	270000 - 277FFF
C	SA86	32K	278000 - 27FFFF
C	SA87	32K	280000 - 287FFF
C	SA88	32K	288000 - 28FFFF
C	SA89	32K	290000 - 297FFF

Memory Organization – 64-Mbit Bottom Boot (Continued)

Plane	Sector	Size (Words)	x16 Address Range (A21 - A0)
C	SA90	32K	298000 - 29FFFF
C	SA91	32K	2A0000 - 2A7FFF
C	SA92	32K	2A8000 - 2AFFFF
C	SA93	32K	2B0000 - 2B7FFF
C	SA94	32K	2B8000 - 2BFFFF
C	SA95	32K	2C0000 - 2C7FFF
C	SA96	32K	2C8000 - 2CFFFF
C	SA97	32K	2D0000 - 2D7FFF
C	SA98	32K	2D8000 - 2DFFFF
C	SA99	32K	2E0000 - 2E7FFF
C	SA100	32K	2E8000 - 2EFFFF
C	SA101	32K	2F0000 - 2F7FFF
D	SA102	32K	2F8000 - 2FFFFF
D	SA103	32K	300000 - 307FFF
D	SA104	32K	308000 - 30FFFF
D	SA105	32K	310000 - 317FFF
D	SA106	32K	318000 - 31FFFF
D	SA107	32K	320000 - 327FFF
D	SA108	32K	328000 - 32FFFF
D	SA109	32K	330000 - 337FFF
D	SA110	32K	338000 - 33FFFF
D	SA111	32K	340000 - 347FFF
D	SA112	32K	348000 - 34FFFF

Memory Organization – 64-Mbit Bottom Boot (Continued)

Plane	Sector	Size (Words)	x16 Address Range (A21 - A0)
D	SA113	32K	350000 - 357FFF
D	SA114	32K	358000 - 35FFFF
D	SA115	32K	360000 - 367FFF
D	SA116	32K	368000 - 36FFFF
D	SA117	32K	370000 - 377FFF
D	SA118	32K	378000 - 37FFFF
D	SA119	32K	380000 - 387FFF
D	SA120	32K	388000 - 38FFFF
D	SA121	32K	390000 - 397FFF
D	SA122	32K	398000 - 39FFFF
D	SA123	32K	3A0000 - 3A7FFF
D	SA124	32K	3A8000 - 3AFFFF
D	SA125	32K	3B0000 - 3B7FFF
D	SA126	32K	3B8000 - 3BFFFF
D	SA127	32K	3C0000 - 3C7FFF
D	SA128	32K	3C8000 - 3CFFFF
D	SA129	32K	3D0000 - 3D7FFF
D	SA130	32K	3D8000 - 3DFFFF
D	SA131	32K	3E0000 - 3E7FFF
D	SA132	32K	3E8000 - 3EFFFF
D	SA133	32K	3F0000 - 3F7FFF
D	SA134	32K	3F8000 - 3FFFFF

Memory Organization – 64-Mbit Top Boot

Plane	Sector	Size (Words)	x16 Address Range (A21 - A0)
D	SA0	32K	00000 - 07FFF
D	SA1	32K	08000 - 0FFFF
D	SA2	32K	10000 - 17FFF
D	SA3	32K	18000 - 1FFFF
D	SA4	32K	20000 - 27FFF
D	SA5	32K	28000 - 2FFFF
D	SA6	32K	30000 - 37FFF
D	SA7	32K	38000 - 3FFFF
D	SA8	32K	40000 - 47FFF
D	SA9	32K	48000 - 4FFFF
D	SA10	32K	50000 - 57FFF
D	SA11	32K	58000 - 5FFFF
D	SA12	32K	60000 - 67FFF
D	SA13	32K	68000 - 6FFFF
D	SA14	32K	70000 - 77FFF
D	SA15	32K	78000 - 7FFFF
D	SA16	32K	80000 - 87FFF
D	SA17	32K	88000 - 8FFFF
D	SA18	32K	90000 - 97FFF
D	SA19	32K	98000 - 9FFFF
D	SA20	32K	A0000 - A7FFF
D	SA21	32K	A8000 - AFFFF
D	SA22	32K	B0000 - B7FFF
D	SA23	32K	B8000 - BFFFF
D	SA24	32K	C0000 - C7FFF
D	SA25	32K	C8000 - CFFFF
D	SA26	32K	D0000 - D7FFF
D	SA27	32K	D8000 - DFFFF
D	SA28	32K	E0000 - E7FFF
D	SA29	32K	E8000 - EFFFF
D	SA30	32K	F0000 - F7FFF
D	SA31	32K	F8000 - FFFFF
C	SA32	32K	100000 - 107FFF
C	SA33	32K	108000 - 10FFFF
C	SA34	32K	110000 - 117FFF
C	SA35	32K	118000 - 11FFFF
C	SA36	32K	120000 - 127FFF
C	SA37	32K	128000 - 12FFFF
C	SA38	32K	130000 - 137FFF
C	SA39	32K	138000 - 13FFFF
C	SA40	32K	140000 - 147FFF
C	SA41	32K	148000 - 14FFFF
C	SA42	32K	150000 - 157FFF
C	SA43	32K	158000 - 15FFFF
C	SA44	32K	160000 - 167FFF

Memory Organization – 64-Mbit Top Boot (Continued)

Plane	Sector	Size (Words)	x16 Address Range (A21 - A0)
C	SA45	32K	168000 - 16FFFF
C	SA46	32K	170000 - 177FFF
C	SA47	32K	178000 - 17FFFF
C	SA48	32K	180000 - 187FFF
C	SA49	32K	188000 - 18FFFF
C	SA50	32K	190000 - 197FFF
C	SA51	32K	198000 - 19FFFF
C	SA52	32K	1A0000 - 1A7FFF
C	SA53	32K	1A8000 - 1AFFFF
C	SA54	32K	1B0000 - 1B7FFF
C	SA55	32K	1B8000 - 1BFFFF
C	SA56	32K	1C0000 - 1C7FFF
C	SA57	32K	1C8000 - 1CFFFF
C	SA58	32K	1D0000 - 1D7FFF
C	SA59	32K	1D8000 - 1DFFFF
C	SA60	32K	1E0000 - 1E7FFF
C	SA61	32K	1E8000 - 1EFFFF
C	SA62	32K	1F0000 - 1F7FFF
C	SA63	32K	1F8000 - 1FFFFF
B	SA64	32K	200000 - 207FFF
B	SA65	32K	208000 - 20FFFF
B	SA66	32K	210000 - 217FFF
B	SA67	32K	218000 - 21FFFF
B	SA68	32K	220000 - 227FFF
B	SA69	32K	228000 - 22FFFF
B	SA70	32K	230000 - 237FFF
B	SA71	32K	238000 - 23FFFF
B	SA72	32K	240000 - 247FFF
B	SA73	32K	248000 - 24FFFF
B	SA74	32K	250000 - 257FFF
B	SA75	32K	258000 - 25FFFF
B	SA76	32K	260000 - 267FFF
B	SA77	32K	268000 - 26FFFF
B	SA78	32K	270000 - 277FFF
B	SA79	32K	278000 - 27FFFF
B	SA80	32K	280000 - 287FFF
B	SA81	32K	288000 - 28FFFF
B	SA82	32K	290000 - 297FFF
B	SA83	32K	298000 -29FFFF
B	SA84	32K	2A0000 - 2A7FFF
B	SA85	32K	2A8000 - 2AFFFF
B	SA86	32K	2B0000 - 2B7FFF
B	SA87	32K	2B8000 - 2BFFFF
B	SA88	32K	2C0000 - 2C7FFF
B	SA89	32K	2C8000 - 2CFFFF

Memory Organization – 64-Mbit Top Boot (Continued)

Plane	Sector	Size (Words)	x16 Address Range (A21 - A0)
B	SA90	32K	2D0000 - 2D7FFF
B	SA91	32K	2D8000 - 2DFFFF
B	SA92	32K	2E0000 - 2E7FFF
B	SA93	32K	2E8000 - 2EFFFF
B	SA94	32K	2F0000 - 2F7FFF
B	SA95	32K	2F8000 - 2FFFFF
A	SA96	32K	300000 - 307FFF
A	SA97	32K	308000 - 30FFFF
A	SA98	32K	310000 - 317FFF
A	SA99	32K	318000 - 31FFFF
A	SA100	32K	320000 - 327FFF
A	SA101	32K	328000 - 32FFFF
A	SA102	32K	330000 - 337FFF
A	SA103	32K	338000 - 33FFFF
A	SA104	32K	340000 - 347FFF
A	SA105	32K	348000 - 34FFFF
A	SA106	32K	350000 - 357FFF
A	SA107	32K	358000 - 35FFFF
A	SA108	32K	360000 - 367FFF
A	SA109	32K	368000 - 36FFFF
A	SA110	32K	370000 - 377FFF
A	SA111	32K	378000 - 37FFFF
A	SA112	32K	380000 - 387FFF

Memory Organization – 64-Mbit Top Boot (Continued)

Plane	Sector	Size (Words)	x16 Address Range (A21 - A0)
A	SA113	32K	388000 - 38FFFF
A	SA114	32K	390000 - 397FFF
A	SA115	32K	398000 - 39FFFF
A	SA116	32K	3A0000 - 3A7FFF
A	SA117	32K	3A8000 - 3AFFFF
A	SA118	32K	3B0000 - 3B7FFF
A	SA119	32K	3B8000 - 3BFFFF
A	SA120	32K	3C0000 - 3C7FFF
A	SA121	32K	3C8000 - 3CFFFF
A	SA122	32K	3D0000 - 3D7FFF
A	SA123	32K	3D8000 - 3DFFFF
A	SA124	32K	3E0000 - 3E7FFF
A	SA125	32K	3E8000 - 3EFFFF
A	SA126	32K	3F0000 - 3F7FFF
A	SA127	4K	3F8000 - 3F8FFF
A	SA128	4K	3F9000 - 3F9FFF
A	SA129	4K	3FA000 - 3FAFFF
A	SA130	4K	3FB000 - 3FBFFF
A	SA131	4K	3FC000 - 3FCFFF
A	SA132	4K	3FD000 - 3FDFFF
A	SA133	4K	3FE000 - 3FEFFF
A	SA134	4K	3FF000 - 3FFFFF

DC and AC Operating Range

		64-Mbit Device – 70, 85 ns
Operating Temperature (Case)	Industrial	-40°C - 85°C
V_{CC} Power Supply		2.7V - 3.6V

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RESET}$	V_{PP}[4]	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	Ai	D_{OUT}
Burst Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	Ai	D_{OUT}
Program/Erase[3]	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IHPP}[5]	Ai	D_{IN}
Standby/Program Inhibit	V_{IH}	X[1]	X	V_{IH}	X	X	High Z
Program Inhibit	X	X	V_{IH}	V_{IH}	X		
	X	V_{IL}	X	V_{IH}	X		
	X	X	X	X	V_{ILPP}[6]		
Output Disable	X	V_{IH}	X	V_{IH}	X		High Z
Reset	X	X	X	V_{IL}	X	X	High Z
Product Identification							
Software				V_{IH}		A0 = V_{IL}, A1 - A21 = V_{IL}	Manufacturer Code[3]
						A0 = V_{IH}, A1 - A21 = V_{IL}	Device Code[3]

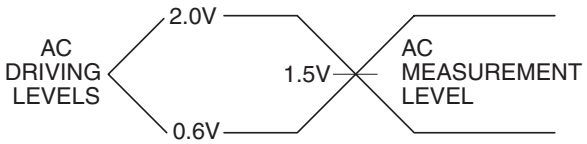
Notes:
1. X can be V_{IL} or V_{IH}.
2. Refer to AC programming waveforms.
3. Manufacturer Code: 001FH; Device Code: 00D6H – Bottom Boot; 00D2H – Top Boot.
4. The VPP pin can be tied to V_{CC}. For faster program/erase operations, V_{PP} can be set to 12.0V ± 0.5V.
5. V_{IHPP} (min) = 1.65V.
6. V_{ILPP} (max) = 0.8V.

DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		1	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		1	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CCQ} - 0.3V to V_{CC}		35	µA
I_{CC}[1]	V_{CC} Active Current	f = 66 MHz; I_{OUT} = 0 mA		30	mA
I_{CCRE}	V_{CC} Read While Erase Current	f = 66 MHz; I_{OUT} = 0 mA		50	mA
I_{CCRW}	V_{CC} Read While Write Current	f = 66 MHz; I_{OUT} = 0 mA		50	mA
V_{IL}	Input Low Voltage			0.6	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA	2.5		V
		I_{OH} = -400 µA	2.4		

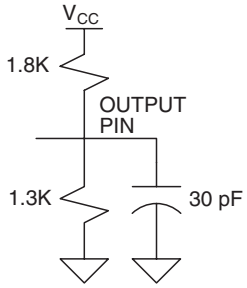
Note: 1. In the erase mode, I_{CC} is 35 mA.

Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

Output Test Load



Pin Capacitance

f = 1 MHz, T = 25°C[1]

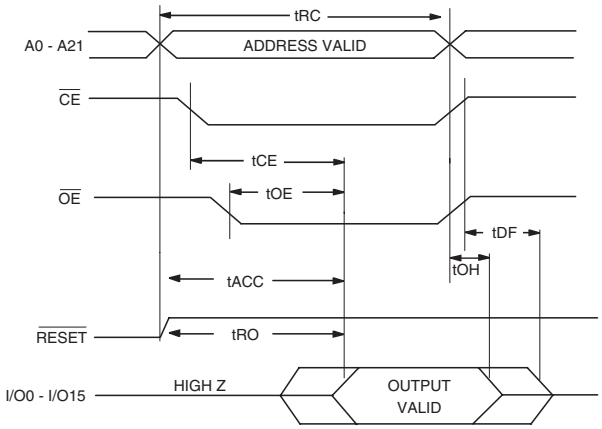
	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

AC Asynchronous Read Timing Characteristics

Symbol	Parameter	64-Mbit-70		64-Mbit-85		Units
		Min	Max	Min	Max	
t_{ACC}	Access, Address to Data Valid		70		85	ns
t_{CE}	Access, $\overline{CE}$ to Data Valid		70		85	ns
t_{OE}	$\overline{OE}$ to Data Valid		20		20	ns
t_{DF}	$\overline{CE}$, $\overline{OE}$ High to Data Float		25		25	ns
t_{RO}	$\overline{RESET}$ to Output Delay		150		150	ns

Asynchronous Read Cycle Waveform(1)(2)(3)



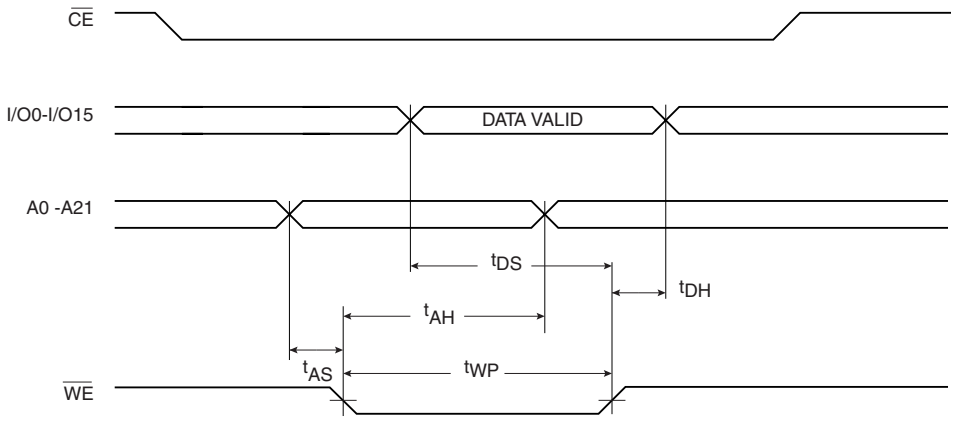
Notes:
1. $\overline{CE}$ may be delayed up to t_{ACC} - t_{CE} after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first (CL = 5 pF).

AC Word Load Characteristics

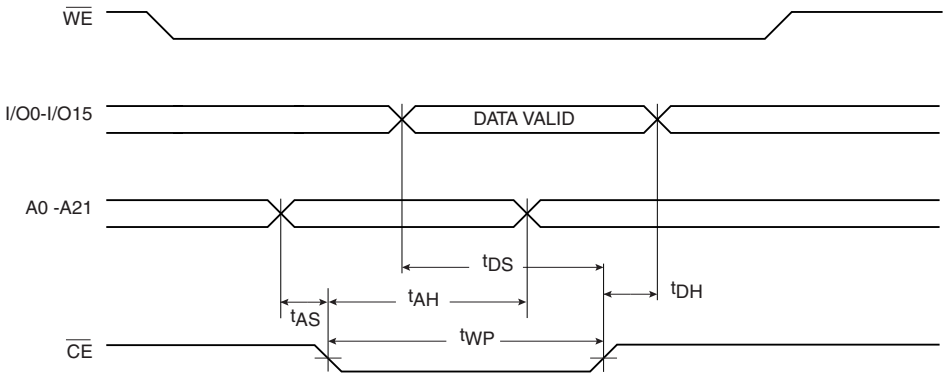
Symbol	Parameter	Min	Max	Units
t_{AS}	Address Setup Time to $\overline{WE}$ and $\overline{CE}$ Low	0		ns
t_{AH}	Address Hold Time	20		ns
t_{DS}	Data Setup Time	20		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	$\overline{CE}$ or $\overline{WE}$ Low Pulse Width	35		ns
t_{WPH}	$\overline{CE}$ or $\overline{WE}$ High Pulse Width	25		ns

AC Word Load Waveforms

$\overline{WE}$ Controlled



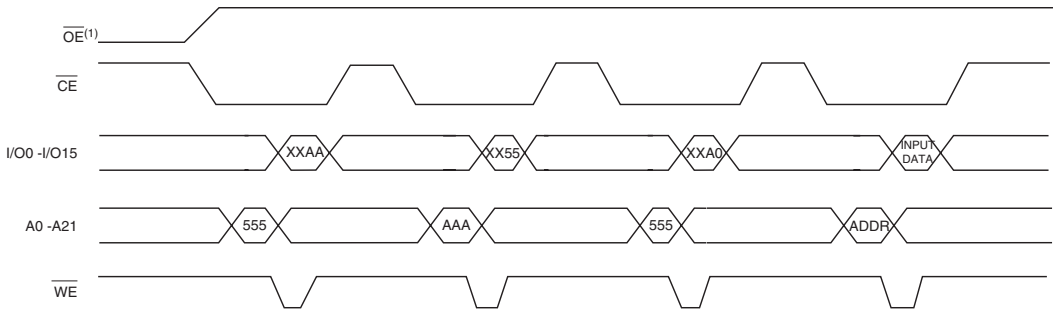
$\overline{CE}$ Controlled



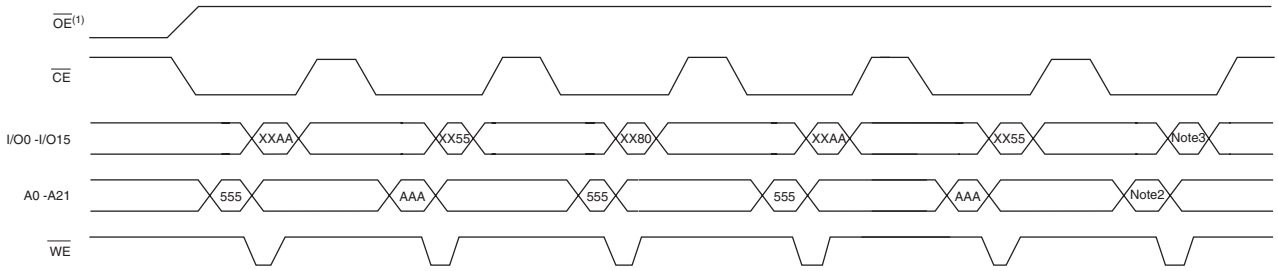
Program Cycle Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{BP}	Word Programming Time ($V_{pp} = V_{CC}$)		22		µs
t_{BPVPP}	Word Programming Time ($V_{PP} \geq 11.5V$)		10		µs
t_{SEC1}	Sector Erase Cycle Time (4K word sectors)		100		ms
t_{SEC2}	Sector Erase Cycle Time (32K word sectors)		500		ms
t_{ES}	Erase Suspend Time			15	µs
t_{PS}	Program Suspend Time			10	µs

Program Cycle Waveforms



Sector, Plane or Chip Erase Cycle Waveforms



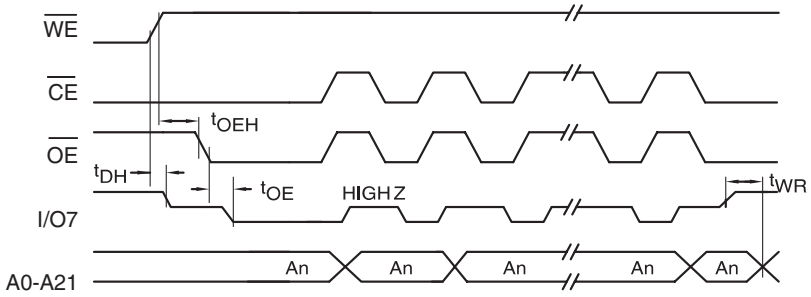
Notes:
1. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.
2. For chip erase, the address should be 555. For plane or sector erase, the address depends on what plane or sector is to be erased. (See note 4 and 6 under Command Definitions on page 12.)
3. For chip erase, the data should be XX10H, for plane erase, the data should be XX20H, and for sector erase, the data should be XX30H
4. The waveforms shown above use the $\overline{WE}$ controlled AC Word Load Waveforms.

$\overline{\text{Data}}$ Polling Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay(2)				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec on page 20.

$\overline{\text{Data}}$ Polling Waveforms

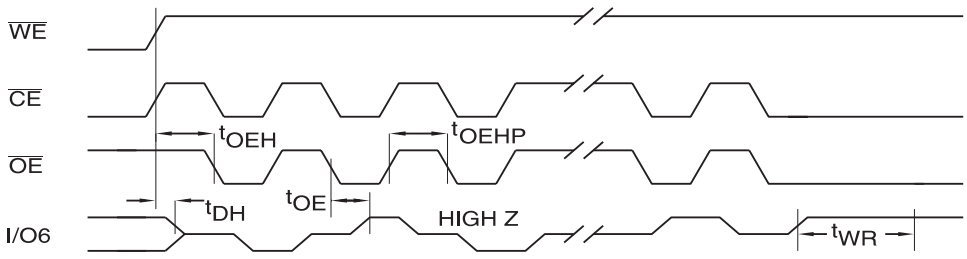


Toggle Bit Characteristics(1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay(2)				ns
t_{OEHP}	$\overline{OE}$ High Pulse	50			ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec on page 20.

Toggle Bit Waveforms(1)(2)(3)



Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
The t_{OEHP} specification must be met by the toggling input(s).
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Table 4. Common Flash Interface Definition for 64-Mbit Device

Address	64-Mbit Device	Comments
10h	0051h	“Q”
11h	0052h	“R”
12h	0059h	“Y”
13h	0002h	
14h	0000h	
15h	0041h	
16h	0000h	
17h	0000h	
18h	0000h	
19h	0000h	
1Ah	0000h	
1Bh	0027h	VCC min write/erase
1Ch	0031h	VCC max write/erase
1Dh	00B5h	VPP min voltage
1Eh	00C5h	VPP max voltage
1Fh	0004h	Typ word write – 16 µs
20h	0000h	
21h	0009h	Typ block erase – 500 ms
22h	0010h	Typ chip erase, 64,300 ms
23h	0004h	Max word write/typ time
24h	0000h	n/a
25h	0003h	Max block erase/typ block erase
26h	0003h	Max chip erase/ typ chip erase
27h	0017h	Device size
28h	0001h	x16 device
29h	0000h	x16 device
2Ah	0000h	Multiple byte write not supported
2Bh	0000h	Multiple byte write not supported
2Ch	0002h	2 regions, x = 2
2Dh	007Eh	64K bytes, Y = 126
2Eh	0000h	64K bytes, Y = 126
2Fh	0000h	64K bytes, Z = 256
30h	0001h	64K bytes, Z = 256
31h	0007h	8K bytes, Y = 7
32h	0000h	8K bytes, Y = 7
33h	0020h	8K bytes, Z = 32
34h	0000h	8K bytes, Z = 32

Table 4. Common Flash Interface Definition for 64-Mbit Device (Continued)

Address	64-Mbit Device	Comments
VENDOR SPECIFIC EXTENDED QUERY		
41h	0050h	“P”
42h	0052h	“R”
43h	0049h	“I”
44h	0031h	Major version number, ASCII
45h	0030h	Minor version number, ASCII
46h	008Fh	Bit 0 – chip erase supported, 0 – no, 1 – yes Bit 1 – erase suspend supported, 0 – no, 1 – yes Bit 2 – program suspend supported, 0 – no, 1 – yes Bit 3 – simultaneous operations supported, 0 – no, 1 – yes Bit 4 – burst mode read supported, 0 – no, 1 – yes Bit 5 – page mode read supported, 0 – no, 1 – yes Bit 6 – queued erase supported, 0 – no, 1 – yes Bit 7 – protection bits supported, 0 – no, 1 – yes
47h	0000h Top Boot or 0001h Bottom Boot	Bit 0 – top (“0”) or bottom (“1”) boot block device Undefined bits are “0”
48h	0000h	Bit 0 – 4 word linear burst with wrap around, 0 – no, 1 – yes Bit 1 – 8 word linear burst with wrap around, 0 – no, 1 – yes Bit 2 – continuos burst, 0 – no, 1 – yes Undefined bits are “0”
49h	0000h	Bit 0 – 4 word page, 0 – no, 1 – yes Bit 1 – 8 word page, 0 – no, 1 – yes Undefined bits are “0”
4Ah	0080h	Location of protection register lock byte, the section's first byte
4Bh	0003h	# of bytes in the factory prog section of prot register – 2*n
4Ch	0003h	# of bytes in the user prog section of prot register – 2*n

16-Mbit PSRAM Description

The device is a 16-Mbit 1T/1C PSRAM featured by high-speed operation and super low power consumption. The 16-Mbit device adopts one transistor memory cell and is organized as 1,048,576 words by 16 bits. It operates in the extended range of temperatures and supports a wide operating voltage range. The device also supports the deep power-down mode for a super low standby current.

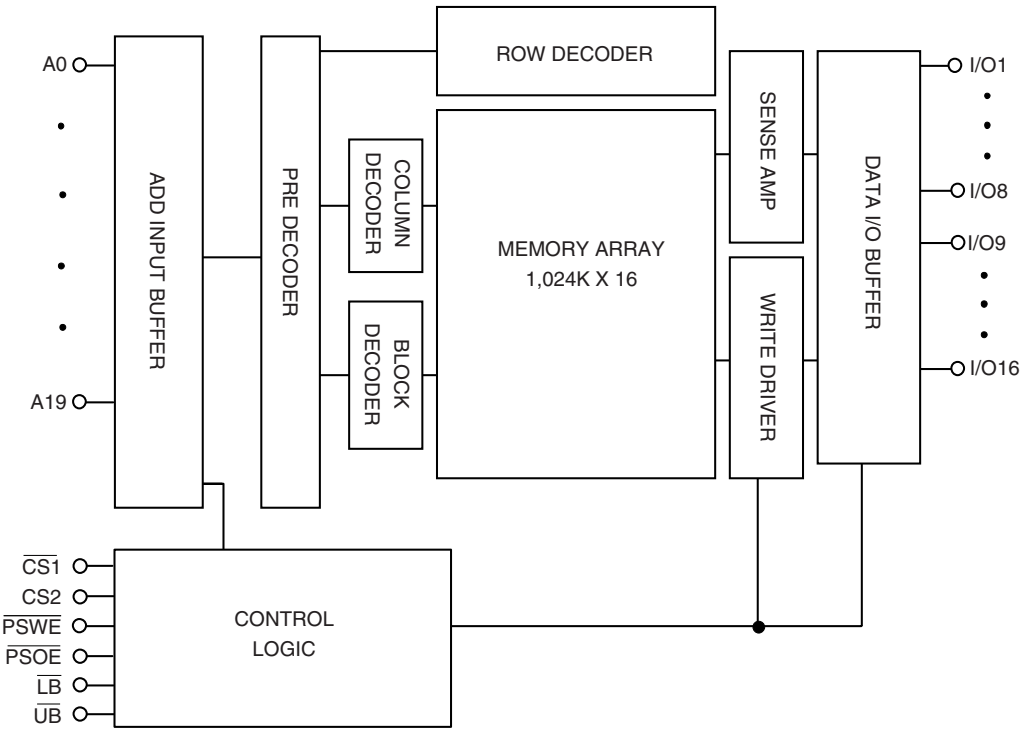
Features

- **CMOS Process Technology**
- **1M x 16-bit Organization**
- **TTL Compatible and Tri-state Outputs**
- **Deep Power-down: Memory Cell Data Hold Invalid**
- **Data Mask Function by $\overline{LB}$, $\overline{UB}$**

Product	Voltage [V]	Mode	Power Dissipation (Max)			Speed t_{RC} [ns]	Temp. [°C]
			(I_{SB1})	(I_{DPD})	(I_{CC2})		
16-Mbit PSRAM	2.7 ~ 3.1	CS1 with $\overline{UB}$, $\overline{LB}$:t_{OE}(1)	85 µA	10 µA	25 mA	70	-30 ~ 85

Note: 1. t_{OE} – $\overline{UB}$, $\overline{LB}$ = High:Output Disable.

Block Diagram



Absolute Maximum Ratings[1]

Symbol	Parameter	Rating	Unit
V_{IN}, V_{OUT}	Input/Output Voltage	-0.3 to V_{CC} +0.3	V
V_{CC}	Power Supply	-0.5 to 3.6	V
T_A	Ambient Temperature	-30 to 85	°C
T_{STG}	Storage Temperature	-55 to 150	°C
P_D	Power Dissipation	1.0	W
T_{SOLDER}	Ball Soldering Temperature and Time	260•10	°C•sec

Note: 1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability.

Truth Table

							I/O Pin		
$\overline{CS1}$	CS2	$\overline{PSWE}$	$\overline{PSOE}$	$\overline{LB}$[2]	$\overline{UB}$	Mode	I/O1 ~ I/O8	I/O9 ~ I/O16	Power
H[1]	H	X	X	X	X	Deselected	High-Z	High-Z	Standby
X[1]	L	X	X	X	X	Deselected	High-Z	High-Z	Deep Power-down
L[1]	H	X	X	H	H	Output Disabled	High-Z	High-Z	Active
L	H	H	H	X	X	Output Disabled	High-Z	High-Z	Active
L	H	H	L	L	H	Lower Byte Read	D_{OUT}	High-Z	Active
L	H	H	L	H	L	Upper Byte Read	High-Z	D_{OUT}	Active
L	H	H	L	L	L	Word Read	D_{OUT}	D_{OUT}	Active
L	H	L	X	L	H	Lower Byte Write	D_{IN}	High-Z	Active
L	H	L	X	H	L	Upper Byte Write	High-Z	D_{IN}	Active
L	H	L	X	L	L	Word Write	D_{IN}	D_{IN}	Active

Notes: 1. H = V_{IH}, L = V_{IL}, X = Don't Care (V_{IL} or V_{IH}).
2. $\overline{UB}$, $\overline{LB}$ (Upper, Lower Byte Enable). These active LOW inputs allow individual bytes to be written or read. When $\overline{LB}$ is LOW, data is written or read to the lower byte, I/O1 - I/O8. When $\overline{UB}$ is LOW, data is written or read to the upper byte, I/O9 - I/O116.

Recommended DC Operating Condition

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	2.7	2.9	3.1	V
GND	Ground	0		0	V
V_{IH}	Input High Voltage	2.2		V_{CC} + 0.3	V
V_{IL}[1]	Input Low Voltage	-0.3[1]		0.6	V

Note: 1. V_{IL} = -1.5V for pulse width less than 10 ns. Undershoot is sampled, not 100% tested.

DC Electrical Characteristics

V_{CC} = 2.7V - 3.1V, T_A = -30°C to 85°C (I)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}	-1	1	µA
I_{LO}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, $\overline{CS1}$ = V_{IH}, CS2 = V_{IH}, $\overline{PSOE}$ = V_{IH} or $\overline{PSWE}$ = V_{IL}	-1	1	µA
I_{CC}	Operating Power Supply Current	$\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, V_{IN} = V_{IH} or V_{IL}, $I_{I/O}$ = 0 mA		3	mA
I_{CC1}	Average Operating Current	$\overline{CS1}$ ≤ 0.2V, CS2 ≥ V_{CC} - 0.2V V_{IN} ≤ 0.2V or V_{IN} ≥ V_{CC} - 0.2V, Cycle Time = 1 µs 100% Duty, $I_{I/O}$ = 0 mA		5	mA
I_{CC2}		$\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, V_{IN} = V_{IH} or V_{IL}, Cycle Time = Min 100% Duty, $I_{I/O}$ = 0 mA		25	mA
I_{SB}	TTL Standby Current	$\overline{CS1}$, $\overline{CS2}$ = V_{IH} or $\overline{UB}$, $\overline{LB}$ = V_{IH}		0.5	mA
I_{SB1}	Standby Current (CMOS Input)	$\overline{CS1}$, CS2 ≥ V_{CC} - 0.2V or		85	µA
I_{DPD}	Deep Power-down Current	CS2 ≤ GND +0.2V		10	µA
V_{OL}	Output Low Voltage	I_{OL} = 0.5 mA		0.3	V
V_{OH}	Output High Voltage	I_{OH} = -0.5 mA	V_{CC} - 0.3		V

Capacitance[1]

(Temp = 25°C, f = 1.0 MHz)

Symbol	Parameter	Condition	Max	Unit
C_{IN}	Input Capacitance (Add, $\overline{CS1}$, CS2, $\overline{PSWE}$, $\overline{PSOE}$, $\overline{UB}$, $\overline{LB}$)	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance (I/O)	$V_{I/O}$ = 0V	10	pF

Note: 1. These parameters are sampled and not 100% tested.

AC Characteristics

V_{CC} = 2.7V ~ 3.1V, T_A = -30°C to 85°C (I), Unless Otherwise Specified

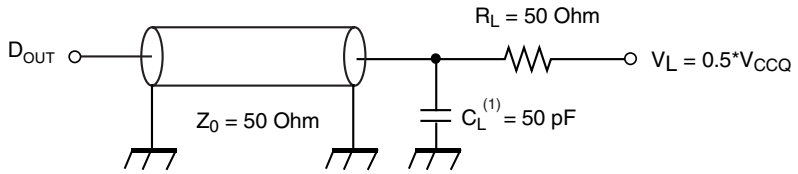
#	Symbol	Parameter	70 ns		Unit
			Min	Max	
Read Cycle					
1	t_{RC}	Read Cycle Time	70		ns
2	t_{AA}	Address Access Time		70	ns
3	t_{ACS}	Chip Select Access Time		70	ns
4	t_{OE}	Output Enable to Output Valid		20	ns
5	t_{BA}	$\overline{LB}$, $\overline{UB}$ Access Time		20	ns
6	t_{CLZ}	Chip Select to Output in Low Z	10		ns
7	t_{OLZ}	Output Enable to Output in Low Z	5		ns
8	t_{BLZ}	$\overline{LB}$, $\overline{UB}$ Enable to Output in Low Z	10		ns
9	t_{CHZ}	Chip Disable to Output in High Z	0	10	ns
10	t_{OHZ}	Out Disable to Output in High Z	0	10	ns
11	t_{BHZ}	$\overline{LB}$, $\overline{UB}$ Disable to Output in High Z	0	10	ns
12	t_{OH}	Output Hold from Address Change	5		ns
Write Cycle					
13	t_{WC}	Write Cycle Time	70		ns
14	t_{CW}	Chip Selection to End of Write	60		ns
15	t_{AW}	Address Valid to End of Write	60		ns
16	t_{BW}	$\overline{LB}$, $\overline{UB}$ Valid to End of Write	60		ns
17	t_{AS}	Address Setup Time	0		ns
18	t_{WP}	Write Pulse Width	50		ns
19	t_{WR}	Write Recovery Time	0		ns
20	t_{WHZ}	Write to Output in High Z	0	20	ns
21	t_{DW}	Data to Write Time Overlap	30		ns
22	t_{DH}	Data Hold from Write Time	0		ns
23	t_{OW}	Output Active from End of Write	5		ns

AC Test Conditions

T_A = -30°C to 85°C (M), Unless Otherwise Specified

Parameter	Value
Input Pulse Level	0.4V to 2.2V
Input Rising and Fall Time	5 ns
Input and Output Timing Reference Level	0.5 * V_{CC}
Output Load	(See AC Test Loads Figure on page 30)

AC Test Loads



Note: Including jig and scope capacitance.

Power-up Sequence

1. Supply power.
2. Maintain stable power for longer than 200 µs.

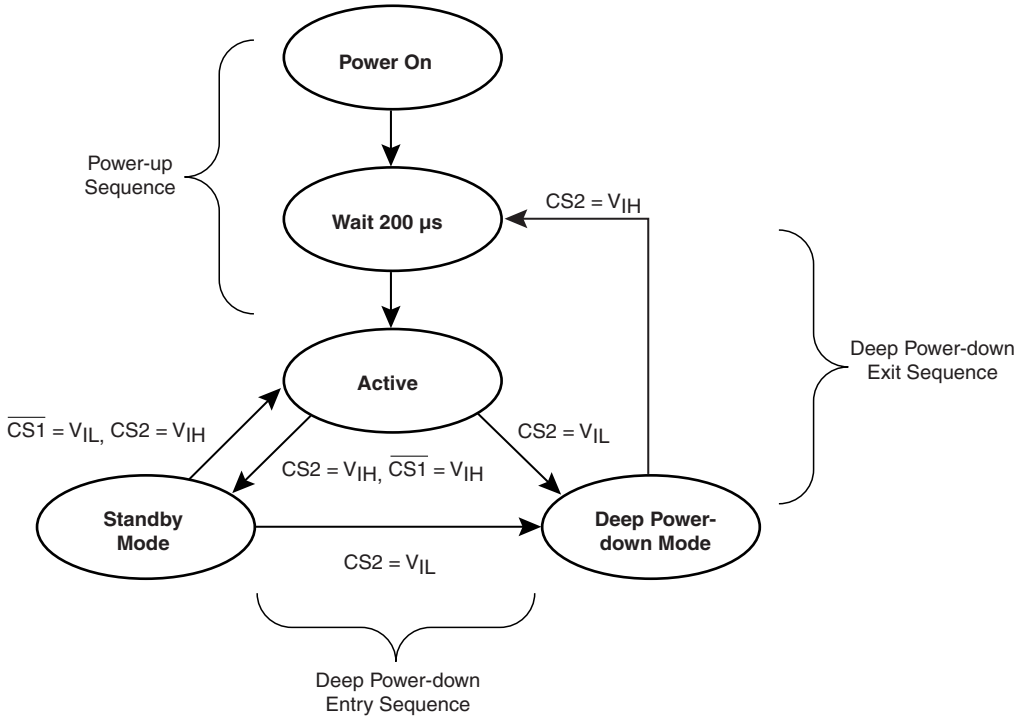
Deep Power-down Entry Sequence

1. Keep CS2 low state. Deep Power-down mode is maintained while CS2 is low state.

Deep Power-down Exit Sequence

1. Keep CS2 high state.
2. Maintain stable power for longer than 200 µs.

State Diagram

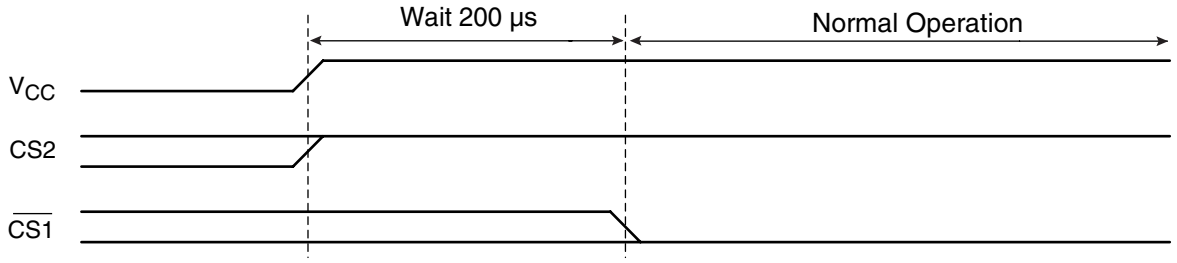


Standby Mode Characteristics

Mode	Memory Cell Data	Standby Current [µA]	Wait Time [µs]
Standby	Valid	85	0
Deep Power-down	Invalid	10	200

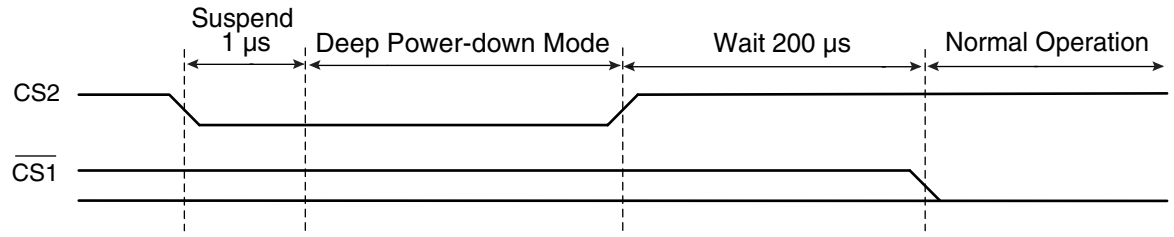
Timing Diagrams

Power-up Sequence Timing



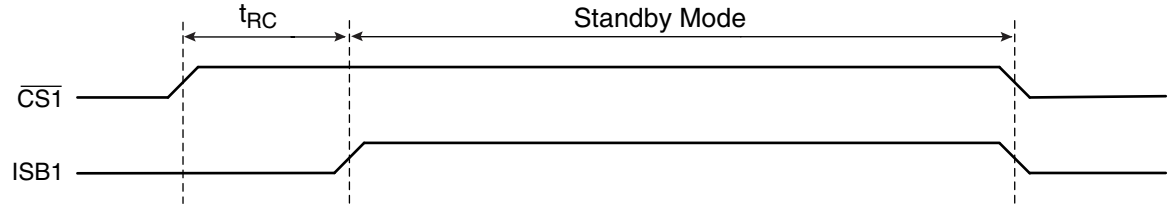
Note: Power-up time is defined when CS2 is kept high before V_{CC} reaches specified minimum level. In case of CS2 is switched from low level to high level, after V_{CC} reached specified level, it is defined as the deep power-down exit.

Deep Power-down Entry/Exit Sequence Timing

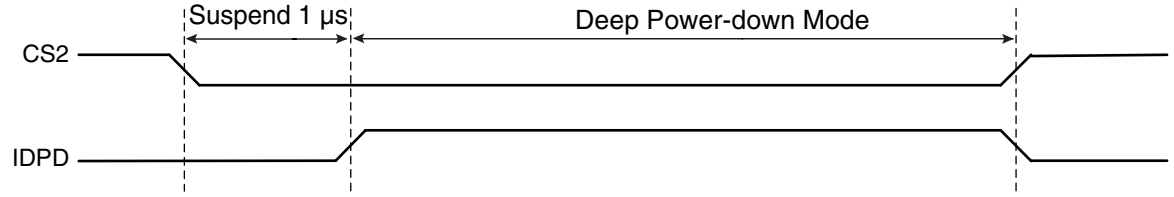


Note: When switching CS2 from high level to low level, the device will be in the deep power-down. In this case, an internal refresh stops and the data might be lost.

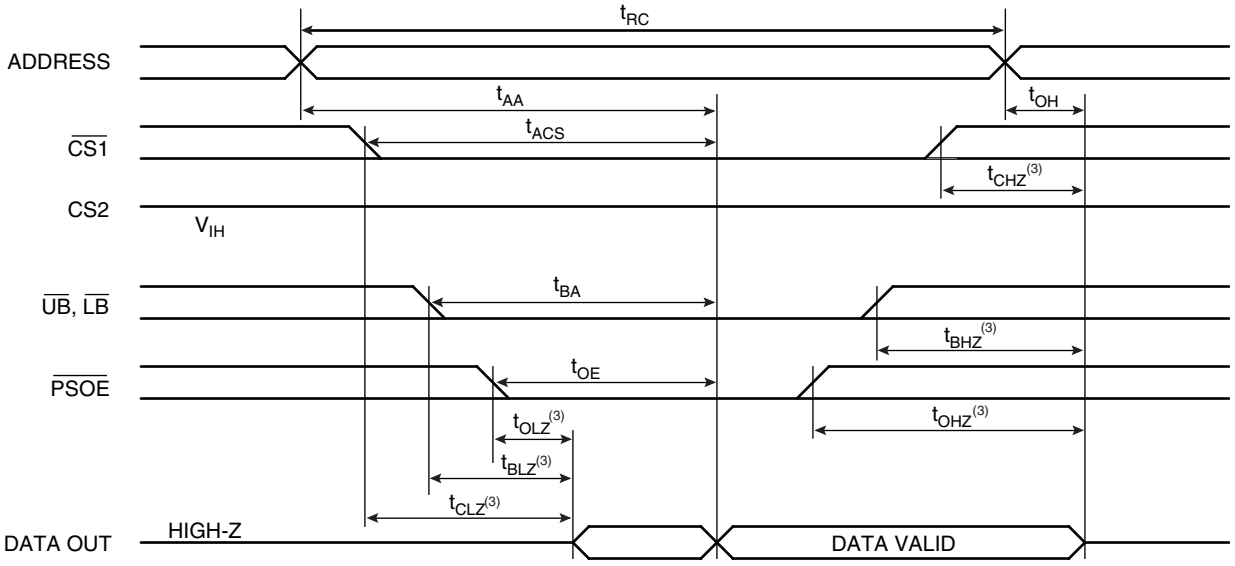
Standby Mode Characteristics Timing



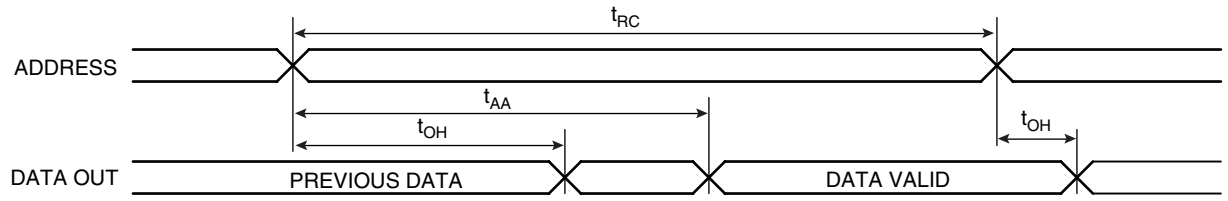
Deep Power-down Mode Characteristics Timing



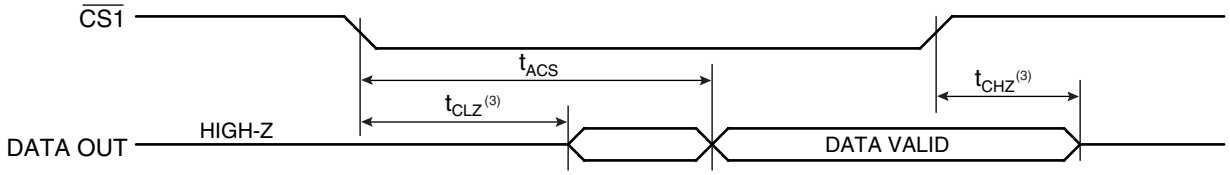
Read Cycle 1[1],[4]



Read Cycle 2, CS2 = V_{IH}[1],[2],[4]

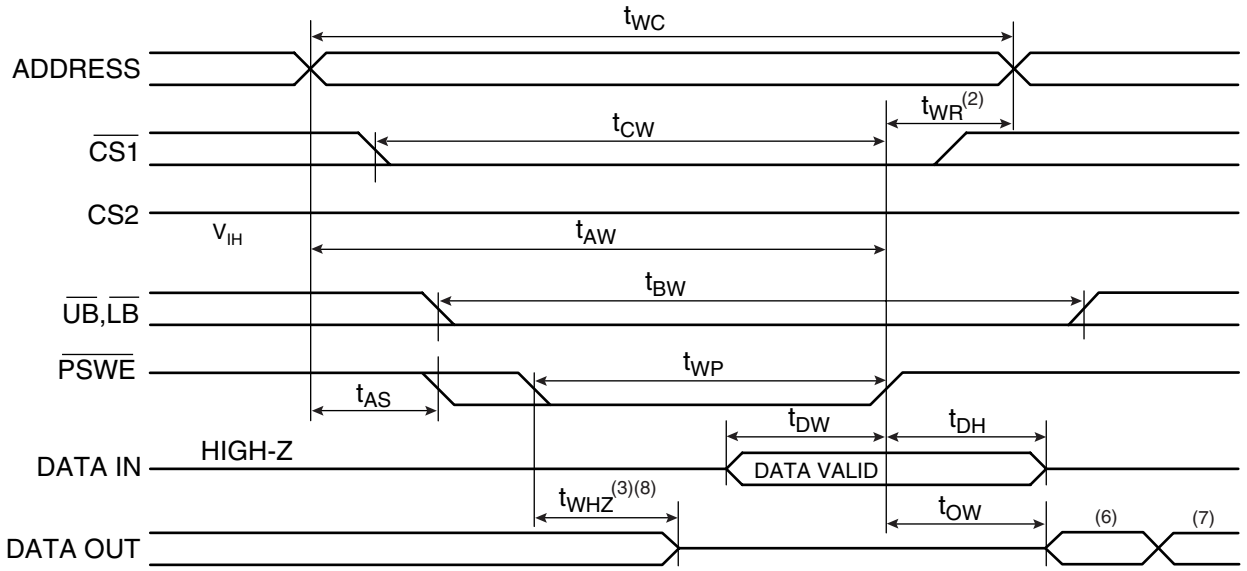


Read Cycle 3, CS2 = V_{IH}[1],[2],[4]

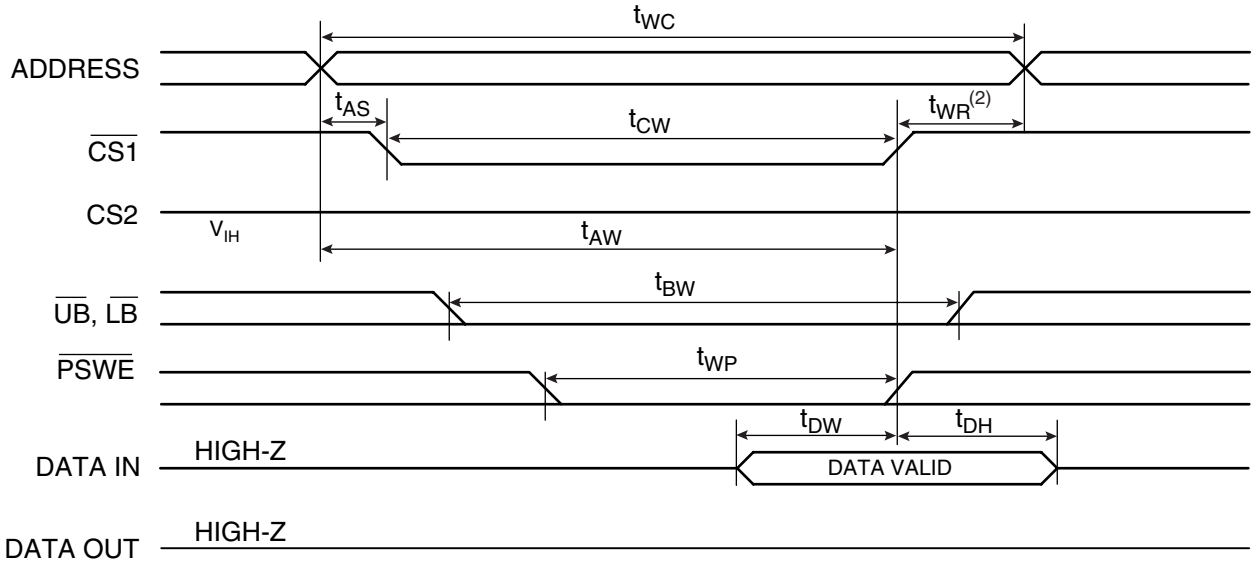


Notes:
1. Read Cycle occurs whenever a high on the $\overline{PSWE}$ and $\overline{PSOE}$ is low, while $\overline{UB}$ and/or $\overline{LB}$ and $\overline{CS1}$ and CS2 are in active status.
2. $\overline{PSOE}$ = V_{IL}.
3. The t_{CHZ}, t_{BHZ} and t_{OHZ} are defined as the time at which the outputs achieve the high impedance state and t_{OLZ}, t_{BLZ} and t_{CLZ} are defined as the time at which the outputs achieve the low impedance state. These are not referenced to output voltage levels.
4. $\overline{CS1}$ in high for the standby, low for active.

Write Cycle 1 ($\overline{PSWE}$ Controlled)(1),(4),(5),(9),(10)

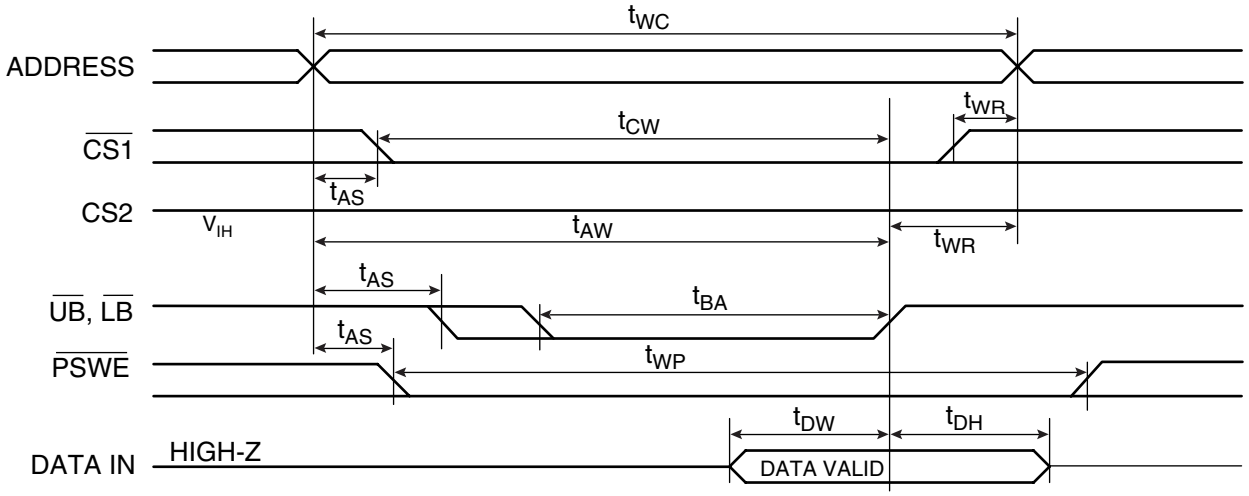


Write Cycle 2 ($\overline{CS1}$ Controlled)(1),(4),(5),(9),(10)



Notes:
1. A write occurs during the overlap of a low $\overline{CS1}$, a low $\overline{PSWE}$, and a low $\overline{UB}$ or $\overline{LB}$.
2. t_{WR} is measured from the earlier of $\overline{CS1}$ or $\overline{PSWE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
4. If the $\overline{CS1}$, $\overline{LB}$ and $\overline{UB}$ low transition occur simultaneously with the $\overline{PSWE}$ low transition or after the $\overline{PSWE}$ transition, outputs remain in a high impedance state.
5. $\overline{PSOE}$ is continuously low ($\overline{PSOE} = V_{IL}$).
6. Q (data out) is the invalid data.
7. Q (data out) is the read data of the next address.
8. The t_{WHZ} is defined as the time at which the outputs achieves the high impedance state. It is not referenced to output voltage levels.
9. $\overline{CS1}$ in high for the standby, low for active.
10. Do not input data to the I/O pins while they are in the output state.

Write Cycle 3 ($\overline{LB}$, $\overline{UB}$ Controlled)

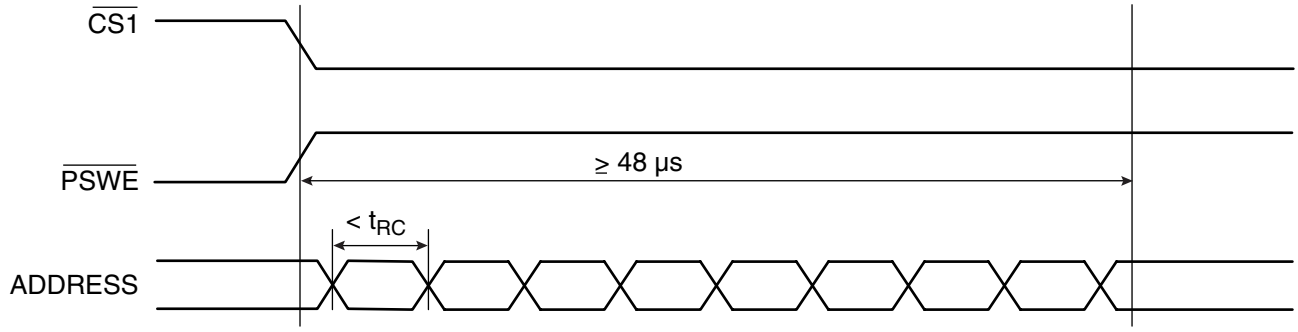


Notes: 1. The t_{BW} is specified from the time satisfied both t_{AS} and t_{WR}.
2. Although $\overline{UB}$ and $\overline{LB}$ are high state, it's illegal function to change address both $\overline{CS}$ and $\overline{PSWE}$ are in low state.

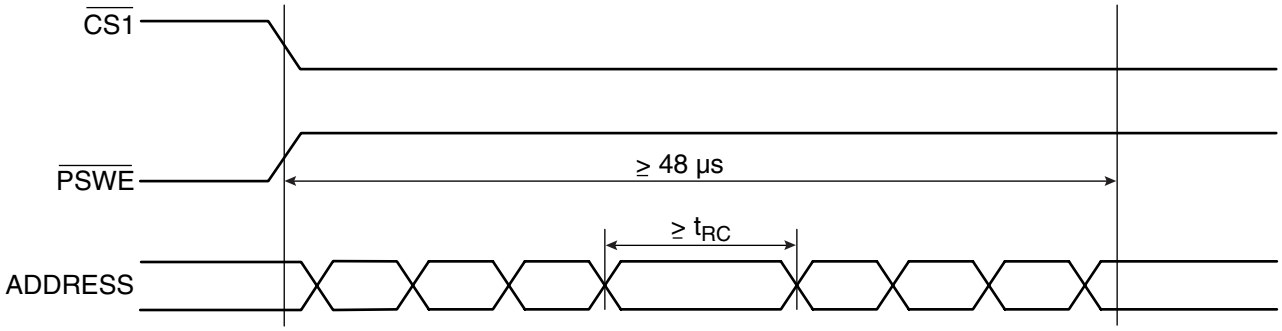
Avoid Timing

The 16-Mbit PSRAM has a timing which is not supported at read operation. If your system has multiple invalid address signal shorter than t_{RC} during over 48 µs at read operation which showed in abnormal timing, it needs a normal read timing at least during 48 µs which showed in Avoidable Timing(1) or toggle the $\overline{CS1}$ to high ($\geq t_{RC}$) one time at least which showed in Avoidable Timing(2)

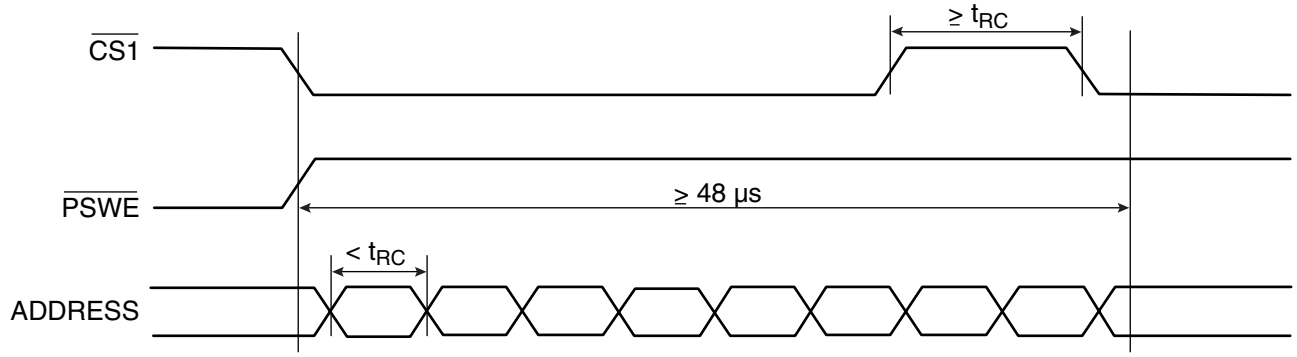
Abnormal Timing



Avoidable Timing (1)



Avoidable Timing (2)



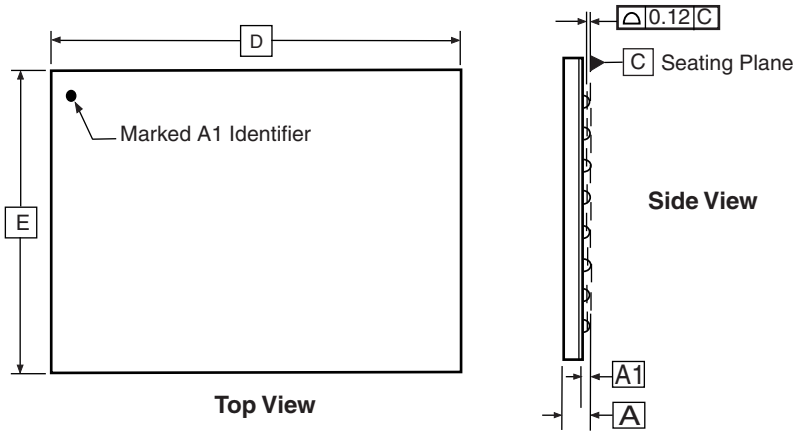
Ordering Information

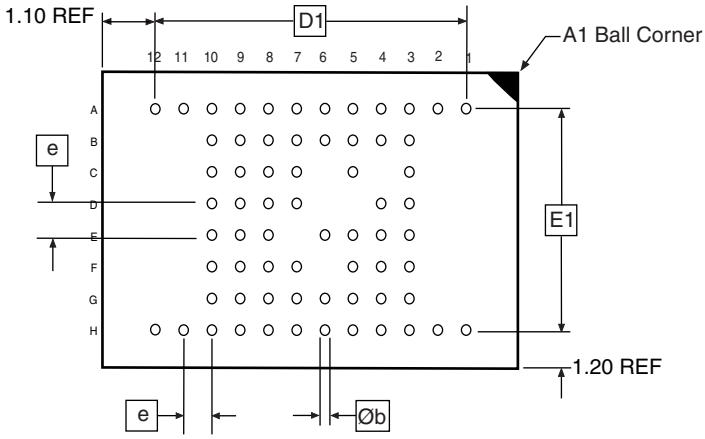
t_{ACC} (ns)	Ordering Code	Flash Boot Block	PSRAM	Package	Operation Range
70	AT52BC6402A-70CI	Bottom	1M x 16	66C6	Industrial (-40° to 85°C)
	AT52BC6402AT-70CI	Top	1M x 16	66C6	Industrial (-40° to 85°C)
85	AT52BC6402A-85CI	Bottom	1M x 16	66C6	Industrial (-40° to 85°C)
	AT52BC6402AT-85CI	Top	1M x 16	66C6	Industrial (-40° to 85°C)

Package Type	
66C6	66-ball, Plastic Chip-size Ball Grid Array Package (CBGA)

Packaging Information

66C6 – CBGA





Bottom View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.0	
A1	0.17	–	–	
D	10.90	11.00	11.10	
D1		8.80 TYP		
E	7.90	8.00	8.10	
E1		5.60 TYP		
e		0.80 TYP		
Øb		0.40 TYP		

08/27/03

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**66C6**, 66-ball (12 x 8 Array), 11 x 8 x 1.0 mm Body, 0.8 mm Ball Pitch Chip-scale Ball Grid Array Package (CBGA)	66C6	A

Atmel Corporation

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