ANSALDO

Ansaldo Trasporti s.p.a.
Unita' Semiconduttori

Via N. Lorenzi 8 - I 16152 GENOVA - ITALY
Tel. int. +39/(0)10 6556549 - (0)10 6556488
Fax Int. +39/(0)10 6442510
Tx 270318 ANSUSE I -

PHASE CONTROL THYRISTOR AT681

Repetitive voltage up to **6000 V**
Mean on-state current **840 A**
Surge current **10 kA**

FINAL SPECIFICATION

feb 97 - ISSUE : 02

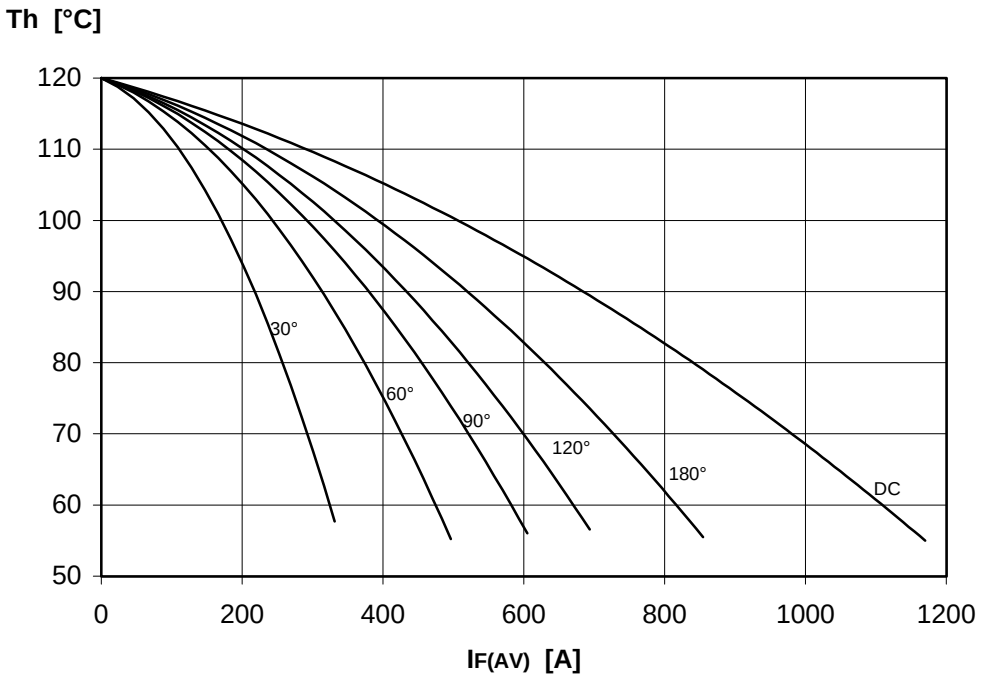
Symbol	Characteristic	Conditions	Tj [°C]	Value	Unit
BLOCKING					
V_{RRM}	Repetitive peak reverse voltage		120	6000	V
V_{RSM}	Non-repetitive peak reverse voltage		120	6100	V
V_{DRM}	Repetitive peak off-state voltage		120	6000	V
I_{RRM}	Repetitive peak reverse current	V=VRRM	120	150	mA
I_{DRM}	Repetitive peak off-state current	V=VDRM	120	150	mA
CONDUCTING					
$I_{T(AV)}$	Mean on-state current	180° sin, 50 Hz, Th=55°C, double side cooled		840	A
$I_{T(AV)}$	Mean on-state current	180° sin, 50 Hz, Tc=85°C, double side cooled		705	A
I_{TSM}	Surge on-state current	sine wave, 10 ms	120	10	kA
I^2t	I^2t	without reverse voltage		500 x1E3	A^2s
V_T	On-state voltage	On-state current = 1570 A	25	2.4	V
$V_{T(TO)}$	Threshold voltage		120	1.3	V
r_T	On-state slope resistance		120	1.150	mohm
SWITCHING					
di/dt	Critical rate of rise of on-state current	From 75% VDRM up to 1200 A	120	100	A/µs
dv/dt	Critical rate of rise of off-state voltage, min.	Linear ramp up to 75% of VDRM	120	500	V/µs
td	Gate controlled delay time, typical	VD=200V, gate source 20V, 10 ohm	25	5	µs
tq	Circuit commutated turn-off time, typical	dV/dt = 20 V/µs linear up to 80% VDRM		650	µs
Q_{rr}	Reverse recovery charge	di/dt=-60 A/µs, I= 1000 A	120		µC
I_{rr}	Peak reverse recovery current	VR= 50 V			A
I_H	Holding current, typical		25	300	mA
I_L	Latching current, typical		25	700	mA
GATE					
V_{GT}	Gate trigger voltage		25	3.5	V
I_{GT}	Gate trigger current	VD=5V	25	400	mA
V_{GD}	Non-trigger gate voltage, min.	0.5 VDRM	120	0.5	V
V_{FGM}	Peak gate voltage (forward)			30	V
I_{FGM}	Peak gate current			10	A
V_{RGM}	Peak gate voltage (reverse)			5	V
P_{GM}	Peak gate power dissipation	Pulse width 100 µs		150	W
P_G	Average gate power dissipation			2	W
MOUNTING					
$R_{th(j-h)}$	Thermal impedance, DC	Junction to heatsink, double side cooled		21	°C/kW
$R_{th(c-h)}$	Thermal impedance	Case to heatsink, double side cooled		6	°C/kW
T_j	Operating junction temperature			120	°C
F	Mounting force			22.0 / 24.5	kN
	Mass			520	g

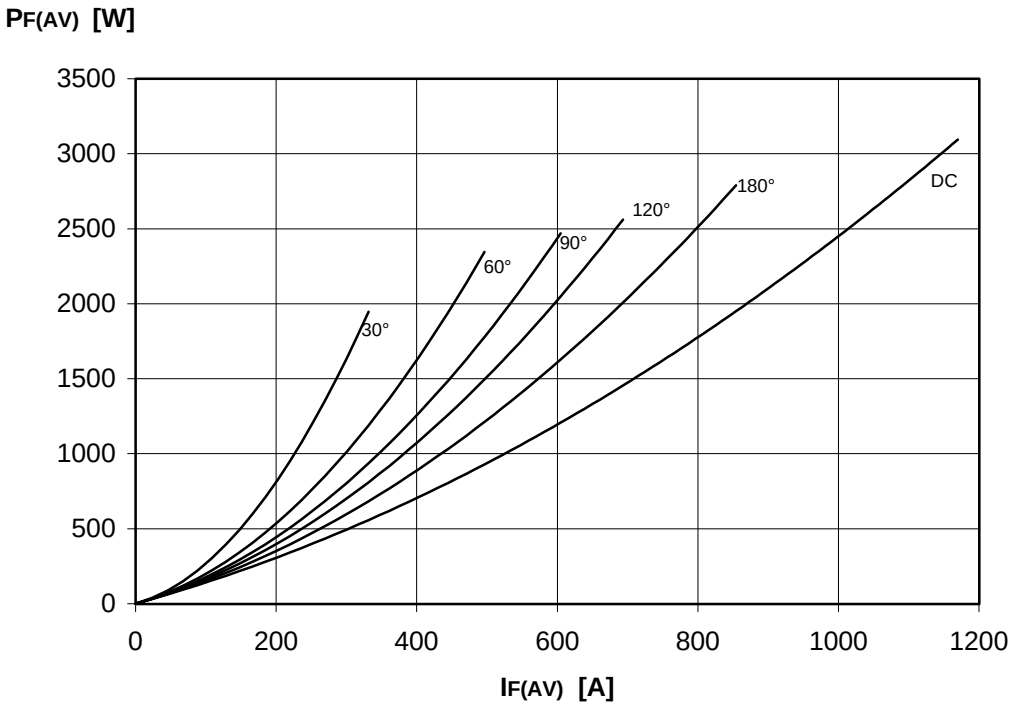
ORDERING INFORMATION : AT681 S 60

standard specification — VDRM&VRRM/100

DISSIPATION CHARACTERISTICS

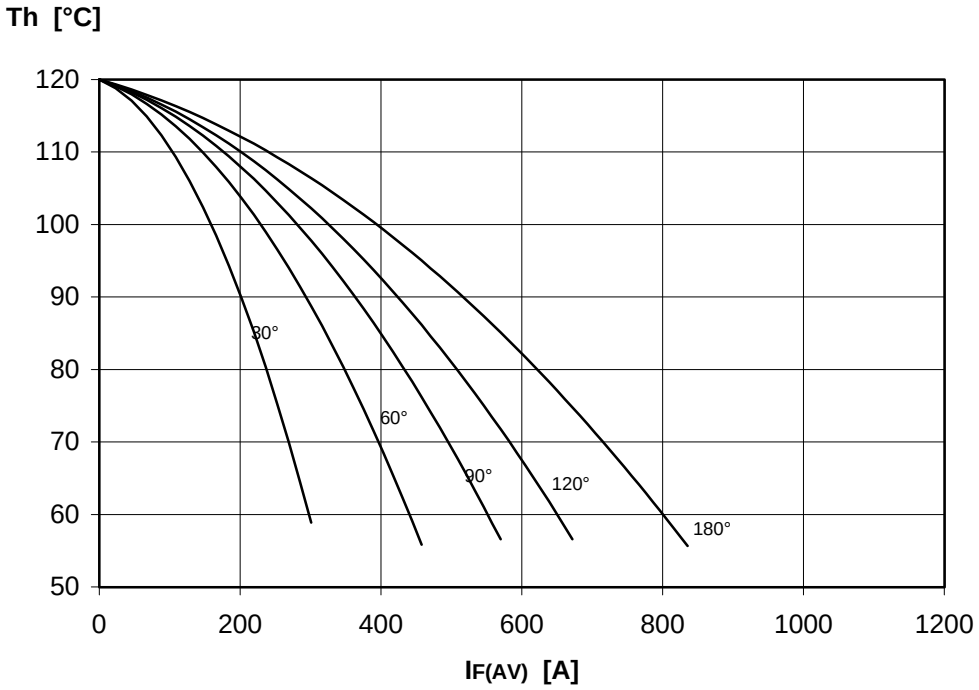
SQUARE WAVE

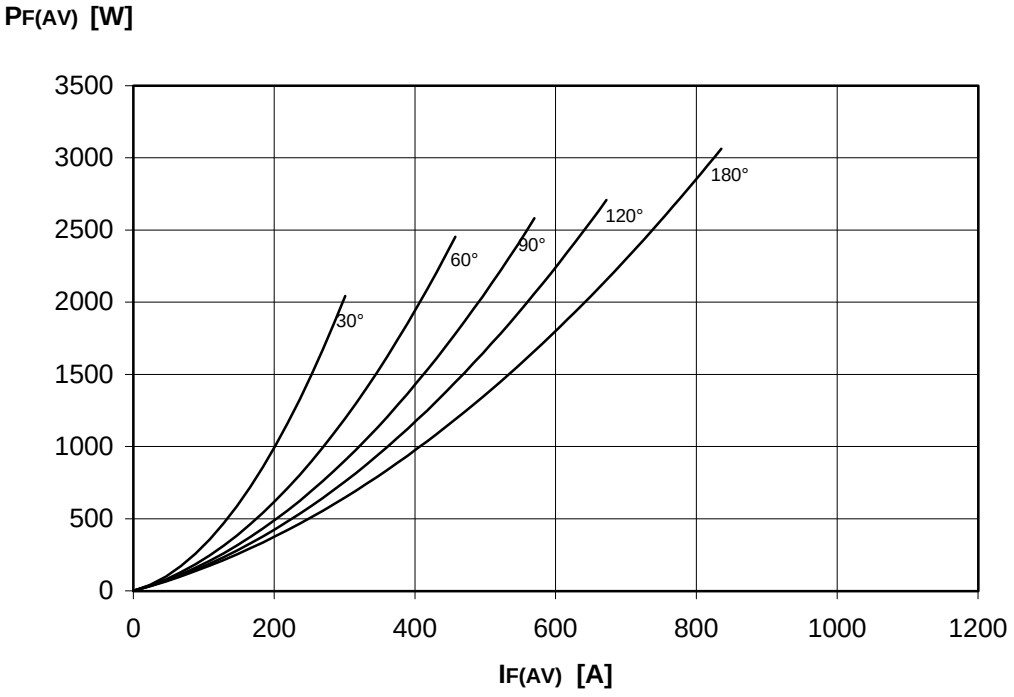




DISSIPATION CHARACTERISTICS

SINE WAVE



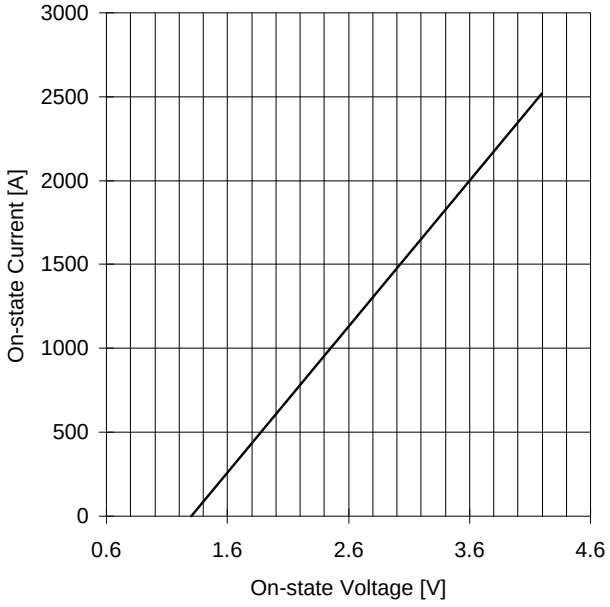


AT681 PHASE CONTROL THYRISTOR

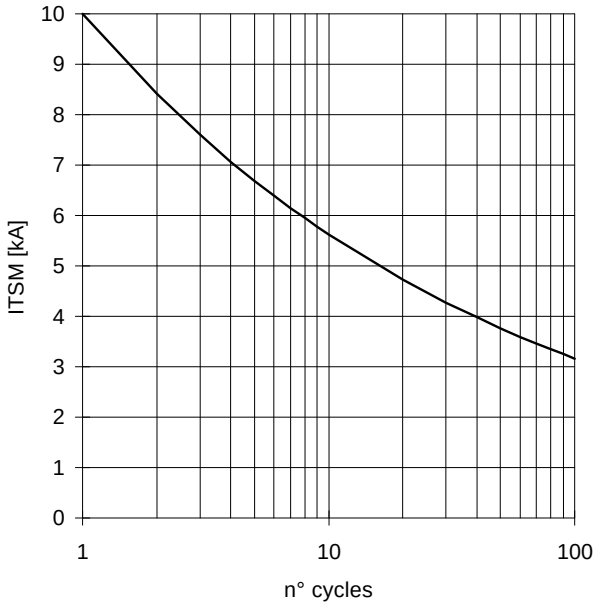
ANSALDO

FINAL SPECIFICATION feb 97 - ISSUE : 02

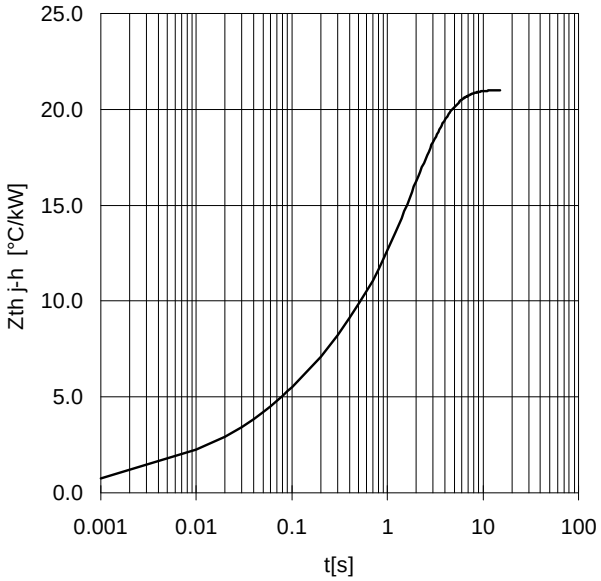
ON-STATE CHARACTERISTIC
Tj = 120 °C

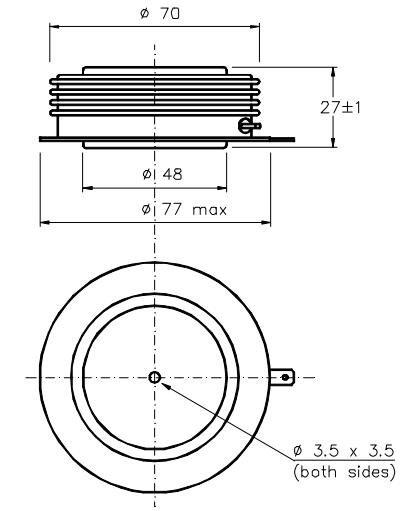


SURGE CHARACTERISTIC
Tj = 120 °C



TRANSIENT THERMAL IMPEDANCE
DOUBLE SIDE COOLED





Dimensions in mm

Cathode terminal type DIN 46244 - A 4.8 - 0.8

Gate terminal type AMP 60598 - 1

All the characteristics given in this data sheet are guaranteed only with uniform clamping force, cleaned and lubricated heatsink, surfaces with flatness < .03 mm and roughness < 2 µm.

In the interest of product improvement ANSALDO reserves the right to change any data given in this data sheet at any time without previous notice.

If not stated otherwise the maximum value of ratings (simbols over shaded background) and characteristics is reported.

Distributed by