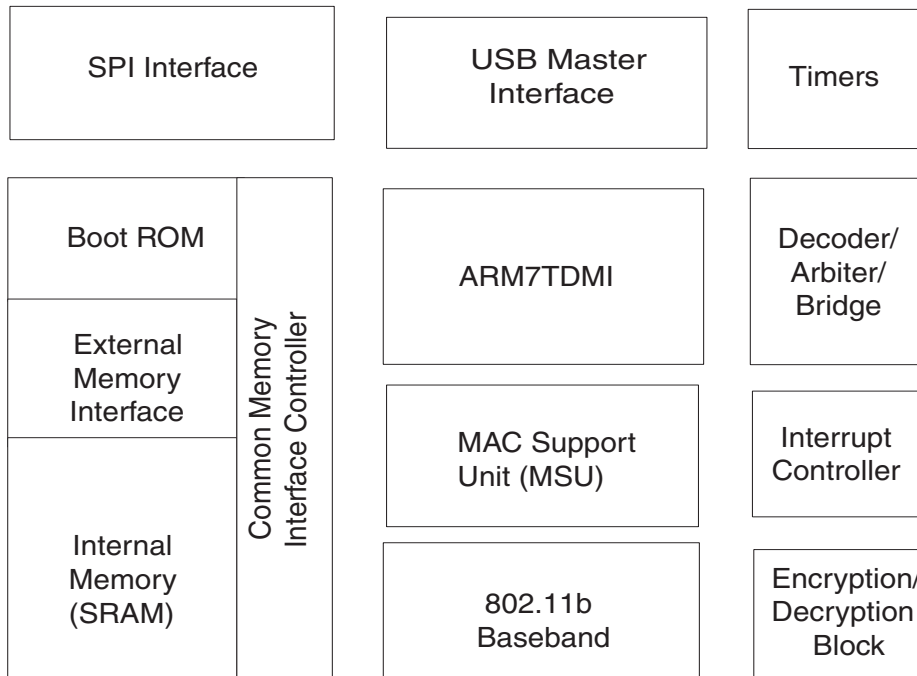


Features

- USB Open Host Controller 1.1 Compliant
- Integrates the IEEE 802.11 Physical Layer (Baseband) and the Medium Access Controller (MAC) for Supporting Standard Rates up to 11 Mbps
- Supports Antenna Diversity Algorithm, Automatic Receive Gain Control, Transmit Gain Control, Transmit Filter for Japanese Regulatory and Differential or Single-ended I- and Q-Baseband Signals
- Integrates 160 KBytes of SRAM Organized in Five Banks of 32 KBytes Each, Offering the Flexibility for Individually Configuring Each of Them as Program or Data Memory
- Zero Wait States for Program Execution
- Fast Data Transfers through DMA Channels
- Low-power ARM7TDMI® RISC Processor
- Integrates a Bootstrap ROM Supporting Firmware Uploading from a Serial DataFlash®
- Glueless Parallel Flash Memory Interface, Supporting up to 128 KBytes of Nonvolatile Memory
- Glueless External SRAM Interface for all MAC Operations, Supporting up to 128 KBytes of External Memory
- Wired Equivalency Privacy (WEP) in Hardware Supporting 64-bit and 128-bit Keys
- Hardware Implementation of TKIP
- Hardware Implementation of AES Encryption Supporting Various Modes (CCM/CTR/CBC)
- The WLAN Functions Can Be Easily Changed or Updated to New Requirements Since They are Implemented in Microcode
- Supports 11 Mbps Rates with Automatic Fallback to 5.5, 2, and 1 Mbps
- SPI Interface and 9 GPIO Pins
- 144-ball LFBGA Package
- Low-voltage 1.8V Operation

Block Diagram



802.11b Media Access Controller (MAC) and Baseband with USB Master Capabilities

AT76C507 Summary

2384AS-WLAN-01/04



Note: This is a summary document. A complete document is available under NDA. For more information, please contact your local Atmel sales office.

Description

The AT76C507 is a single-chip baseband controller that can handle IEEE 802.11b standard compliant data rates of up to 11 Mbps and provides all processing and functionality needed for the MAC protocol of IEEE 802.11b.

The AT76C507 incorporates a USB Open Host Controller (OHC), which is capable of processing all of the data type lists. The OHC has four states, which define its responsibilities relating to USB signaling and bus states. It is also responsible for managing all aspects of framing for the USB. These responsibilities include sending SOF Tokens on the bus and communicating with the Host Controller Driver on frame-specific information. Because the USB does not provide a mechanism for attached devices to arbitrate for granting the bus, arbitration is predictive with the Host Controller. USB by necessity supports a number of different communication models between software and endpoints (Bulk, Control, Interrupt and Isochronous). The usage of the bus varies by the type of service. The approach used by the Host Controller is to have two levels of arbitration to select among the endpoints. The first level of arbitration is at the list level. Each endpoint type needing service is in a list of a corresponding type and the Host Controller selects which list to service. Within a list, endpoints are given equal priority insuring that all endpoints of a certain type have more or less equal service opportunities. The AT76C507 provides two USB Full-Speed (12 Mbits) ports.

Besides the USB interface, the AT76C507 contains a WEP/TKIP engine block, an AES engine block, a MAC Support Unit (MSU), a 802.11b Baseband controller, two memory controllers and the ARM® subsystem consisting of an Interrupt Controller, two 32-bit timers and an address decoder unit.

The ARM7TDMI core supports two alternative instruction sets. Powerful 32-bit code can be executed by the processor in ARM operating mode. However, a 16-bit instruction subset is also available in Thumb® mode. Thumb mode can be selected to exploit full processor power with limited external memory resources. Note that ARM7TDMI operating mode can be changed at run time with negligible overhead.



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