Features

- **13.56 MHz ± 7 kHz RFID Interface for Multi-chip Cards and Tags**
- **Electrically Compatible with ISO/IEC 14443-2, Type B**
- **Serial Channel Configurable to Communicate with External Chips**
- **Supports SPI and Two-wire Serial EEPROM Interface**
- **320 Read/Write EEPROM Bits, Divided into 10 Pages of 32 Bits**
- **Password and Write Lock Protection**
- **Programmable Send Protocols**
- **Integrated Tuning Capacitor**
- **ID Length Programmable from 4 to 18 Bytes**
- **Optional 2-byte CRC**

RFID External EEPROM Interface IC

AT88RF001

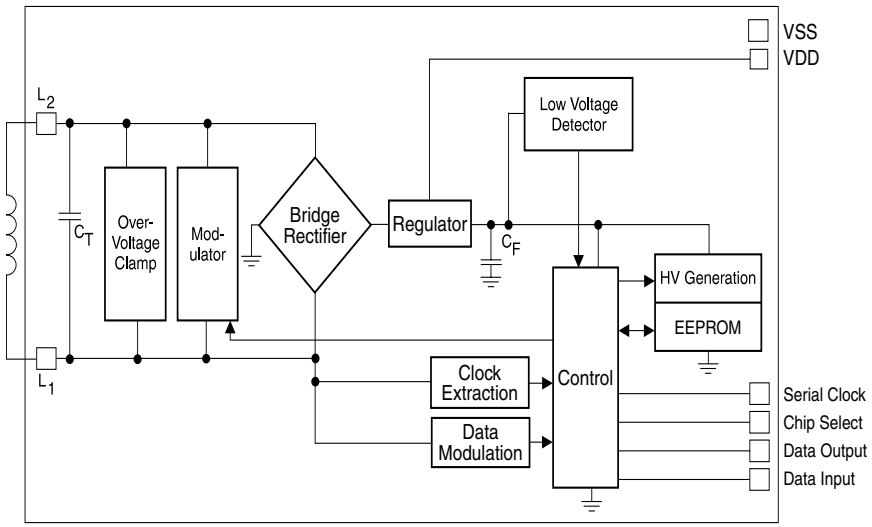
Description

The AT88RF001 is a stand-alone 13.56 MHz RFID front end that includes a serial port suitable for connection to an external high-density serial memory. Using the on-board EEPROM, it can be configured to communicate using various protocols and interface to both two-wire and SPI external devices.

The device contains 320 bits of full read/write EEPROM memory and offers features such as passwords, locking and a variable-length ID. It is electrically compatible with ISO/IEC 14443-2, Type B. The IC includes an internal tuning capacitor; only an external coil antenna is required to complete the RFID channel.

The serial channel is configurable to communicate with external ICs using either two-wire or four-wire (SPI) serial channels, at a maximum speed of 106 kilobits per second (Kbps). An external bypass capacitor will be required to filter and stabilize the supply generated by the RFID front end. Up to 2 mA can be drawn by the external memory when communications are not occurring.

Figure 1. Block Diagram



The AT88RF001 is intended to be used with serial EEPROMs such as Atmel's AT24Cxx two-wire line or its AT25xx SPI line. In addition, it can communicate with an external microprocessor if more complicated systems are to be built, if software on that processor can model the slave protocol of the corresponding memories. It is expected that a single external memory chip will be connected to the AT88RF001.

Rev. 1943F–RFID–04/02

General Operation

On power-up, the device will continuously repeat through the following sequence, which includes an ID transmission and possible reception of a command. The sequence is defined as follows:

1. Framed transmission of the ID field:
   - Start of Transmission (see *Data Communications,* page 6)
   - Between 4 and 18 bytes from the EEPROM, which is defined as the ID field
   - Optional 2-byte CRC
   - End of Transmission (see *Data Communications,* page 6)
2. A listening window, during which commands may be sent to the IC

All bits are sent to or read from the IC least significant bit first. Bit fields listed in this document are listed with the LSB on the left and the MSB on the right.

Multi-byte information is sent to the IC least significant byte first. Although not visible to the external system, within the IC, the first byte sent to the device is stored in memory at the lowest address and the address is incremented for subsequent bytes.

Information is read from the EEPROM and transmitted by the IC in exactly the same order in which it was written: the first bit written is the first bit read.

Information for the external I/O channel is transferred in the same order in which it is transferred along the RFID channel.

ID Field

The ID sent by the IC can be between 4 and 18 bytes in length, depending on the value of the PU_LEN field in the configuration page. EEPROM bytes not utilized for ID storage may be used by the system for any other purpose.

Listening Window

After the power-up sequence is transmitted, there is a listening window during which the tag looks for modulation that would initiate the transmission of a command from the reader/writer to the tag. Commands sent at any other time are ignored.

The listening window is 8 bit-times long. The leading modulation edge of the SOT identifier (see *Data Communications*, page 6) must not start within the first and/or last bit time of the listening window. This restriction is enforced to prevent the IC receiver from seeing its own modulation.

Command Bytes

The internal memory commands implemented in this tag permit the reader/writer to directly access individual 4-byte pages within the internal memory array, prevent future writing of particular pages (locking), temporarily disable the IC, or check a password value. The external memory commands provide a channel for the reader to communicate with the external memory through the RFID channel. In the event that the device does not acknowledge the Check Password, Send Begin, Send End, Send Byte, or Send Page commands, then the operation failed. The reader should wait 10 bit-times from the time when the AT88RF001's SOT was supposed to start before issuing another command.

These commands are encoded as follows:

LSB MSB	Command
A_0 A_1 A_2 A_3 0 0 0 1	Read 32-bit Page A A A A (followed by optional CRC)
A_0 A_1 A_2 0 0 0 1 0	Write 32-bit Page A A A (followed by 4 bytes of data and optional CRC)
0 0 0 0 0 0 1 1	Write Lock Byte (followed by 1 byte of data, 3 bytes of $AAH and optional CRC)
0 0 0 1 0 0 1 1	Write Configuration Bits (followed by 1 byte of $AAH, 3 bytes of data and optional CRC)
0 0 0 0 0 1 1 1	Write Password (followed by 4 bytes of data and optional CRC)
0 0 0 1 1 0 0 0	Disable (Stop) IC until Power-down (followed by optional CRC)
0 0 0 1 1 1 0 0	Check Password (followed by 4 bytes of data and optional CRC)
0 0 1 0 0 0 1 1	Send Byte to I/O Channel (followed by 1 byte of data and optional CRC)
0 0 1 0 0 1 1 1	Get Byte from I/O Channel (followed by optional CRC)
0 0 1 0 1 0 1 1	Send Page to I/O Channel (followed by # of bytes determined by PAGE_SIZE, CRC)
0 0 1 0 1 1 1 1	Get Page from I/O Channel (followed by optional CRC)
0 1 0 0 0 0 1 1	Send Begin Sequence to I/O Channel (CS low or START)
0 1 0 0 0 1 1 1	Send End Sequence to I/O Channel (CS high or STOP)
0 1 0 0 1 1 1 1	Send End Sequence to I/O Channel, Wait 6 ms (CS high or STOP)
0 1 0 1 0 1 1 1	Send End Sequence to I/O Channel, Wait 11 ms (CS high or STOP)
0 1 0 1 1 1 1 1	Send End Sequence to I/O Channel, Wait 21 ms (CS high or STOP)

Internal EEPROM Access

For the Read and all four Write commands, the data stored within the corresponding page of the EEPROM is repeatedly transmitted back to the reader by the IC after the command has completed. This permits a verify function for the commands. For the Write Lock and Write Config commands, the entire contents of page 8 are transmitted. Between each frame transmitted, there is a listening window of 8 bit-times to synchronize the reader and/or permit the reader/writer to issue a new command to the IC. The listening window will begin immediately following the transmission of the appropriate EOT (see *Data Communications* section for information regarding EOT).

External Memory Access

The Send and Get commands transfer data from the RFID port to the serial I/O channel bit by bit, using the proper protocol for the external memory as defined by the SERIAL_MODE bits in the options page. The Send/Get Page commands transfer a number of bytes as set in the options page, which could correspond to the page size in the external memory. Any sequencing required in the external memory to perform writes or other housekeeping should be performed with a series of Send/Get commands, either as single bytes or as combinations of byte and page commands.

All Send/Get data commands to the external memory should be preceded with a start sequence that is initiated with the Send Begin command. External memory operations should be terminated with the Send End command. In two-wire mode, these commands correspond to the start and stop conditions. In SPI mode, the Begin/End commands assert and deassert the CS pin to the external memory.

If extra security is required before access to the external memory, the IC can be configured such that the password must be entered before the Send Begin command will be executed. Without this command being executed, accesses to the external memory cannot happen.

After any Send, Get or Check Password command has properly executed, the IC enters an infinite listening window during which additional commands can be sent to the IC. After subsequent Send, Get or Check Password commands have been executed and/or if illegal commands are sent to the device, it will return to this infinite listening window.

After subsequent internal memory access commands have been executed, the IC will acknowledge the command by repeatedly transmitting the page accessed. Subsequent illegal commands will result in the power-up ID transmission.

After any Send command that is received correctly (including encoding and/or CRC) and acknowledged by the external memory, the IC will send a single-byte acknowledge frame back to the reader in the form of a single byte of value 0xFF (and CRC, if enabled).

In the case of the Send Begin/Send End commands, the absence of an acknowledge response from the IC means that the various pin transitions to the external memory did not occur at all. In the case of the other external memory access commands, the IC will stop transitions to the external memory at the point of failure, and the reader must determine the proper course of action to recover the external memory state.

After the Send End command is initiated, the command encoding may specify that a delay occurs after the acknowledge is sent back to the reader. Because of the architecture of the power generation circuitry, it is recommended that these delays be used whenever writes will be taking place within the external memory. During the delay time, the IC will be configured to supply extra power to the external memory device, and communications to the AT88RF001 will be disabled during the delay period.

The system can send any command (either external or internal memory access) during any listening window. To return to the default state and transmit the ID, the carrier power can be cycled off and on.

Write Protection

There are a number of features that are used to prevent inadvertent writing of the device:

1. The proper command code plus the proper receive data encoding must be sent to the IC. If either an illegal code or improper encoding is detected, the command is aborted.
2. Optionally, 2 CRC bytes may be sent after the command and data bytes (see below for details), which must also be correct.
3. For the Write Lock command, a successful Write Page command must have been previously executed since the last power cycle in order for the Write Lock command to be executed.

If any of these protections are violated, or if there is a transmission or protection failure (lock bit set, password not entered), or if an illegal command is sent, the internal EEPROM will not be written.

Data Locking

Within the lock byte, each lock bit determines whether the corresponding 4-byte user page can be written to. If it contains a “1”, then writes are prohibited; if “0”, they are allowed. The data sent to the IC with the Write Lock operation is ORed with the data already in the lock byte and then rewritten to the EEPROM. Once a user page is locked, it may never be unlocked and may never be written to.

There are two additional lock bits for pages 8 (CONFIG_LOCK) and 9 (PW_LOCK). They operate slightly differently from the user lock bits because there is no OR function. CONFIG_LOCK, if “1”, prevents the execution of the Write Config Bits command, while PW_LOCK, if “1”, prevents execution of the Write Password command. Turning on CONFIG_LOCK does not lock the value of the bits within the lock byte but does prevent further change to the PW_LOCK bit and the other configuration bits.

Passwords

If the optional password mode is enabled with PW_ON, command-based reads and writes are prohibited until the correct password is sent using the Check Password command. If the transmitted value of the password is correct, then an internal latch is set and subsequent Read, Write and Lock commands (to any page, including the password page, #9) are permitted. If the wrong password is sent (to the password check), then the command is aborted. Writes to locked pages are never permitted regardless of passwords.

If PW_EXT is set to “1”, then the Send Begin command may not be executed until the correct password has been sent to the IC using the Check Password command. The state of PW_ON does not affect whether or not the password is required to execute the Send Begin command.

There is no command that can be used to directly read the password page, regardless of whether or not the password option (PW_ON or PW_EXT) is enabled.

Simple I/O Mode

When the IC is configured for simple I/O mode, the state of two output pins can be controlled by the reader, and the state of two input pins can be determined by the reader. To enable this mode, SERIAL_MODE should be set to the “simple I/O” state.

When the Send Byte command is executed, bit 0 of the data will be driven to the SCK pin and bit 1 of the data will be driven to the CS pin. Bits 2–7 are ignored. When the Get Byte command is executed, bit 0 will reflect the current state of the SO pin and bit 1 will reflect the state of the SI pin. Bits 2–7 will be 0.

The current state of the pins are stored in CMOS latches and are not saved across power cycles. When simple I/O mode is enabled, on power-up and if the IC is reset, the output pins are driven high.

The Send/Get Page commands and the Begin/End commands are disabled when in this mode. If the external devices drive the input pins away from the supply rails by more than 0.6V, the IC will consume additional current and may malfunction.

Data Communications

The electrical signaling of the IC can be modified using the DATA_ENCODE bit in the configuration page. One state of this option supports compatibility with ISO/IEC 14443-2 Type B “Radio frequency power and signal interface” (version N409, Final Committee Draft 3/12/99). The frame formatting for the various modes of operation is not fully compliant with ISO/IEC 14443-3 and is defined below.

Electrical Signaling

The DATA_ENCODE bit within the configuration page bit determines the outgoing (IC to reader/writer) data encoding format.

0 – selects BPSK-NRZ-L, which is compliant with ISO/IEC 14443-2, Type B. When BPSK-NRZ-L is selected, the subcarrier is modulated with the carrier. A 180° phase change of the subcarrier occurs whenever the data state changes.

1 – selects BPSK-Miller encoding. When BPSK-Miller is selected, the subcarrier is modulated with the carrier. For a logic “1”, a 180° phase transition of the subcarrier will occur in the middle of the bit time. For a logic “0” following a logic “1”, there will be no phase change of the subcarrier during the bit time. For a logic “0” following a logic “0”, there will be a 180° phase change of the subcarrier at the beginning of the bit time.

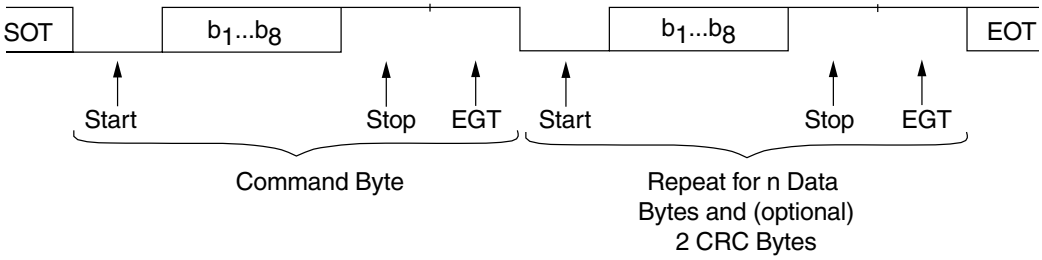
Type B Frame Mode

All commands and data sent to the IC shall be received in the following format:

1. Start of Transmission (SOT) (see below for Type B SOT definition).
2. One command byte (1 logic “0” start bit + 8 command bits + 1 logic “1” stop bit + EGT(1)).
3. N data bytes: N*(1 logic “0” start bit + 8 data bits + 1 logic “1” stop bit + EGT(1)) N ≥ 0.
4. (Optional) Two CRC bytes in the same format as above (3).
5. End of Transmission (EOT) (see below for Type B EOT definition).

Note: 1. The EGT (Extra Guard Time) is an integer of 0–6 additional logic “1”s transmited after the stop bit.

Figure 2. Type B Frame Format – Reader/Writer to Card

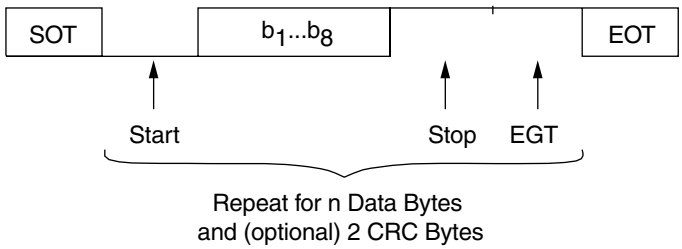


All data sent from the IC to the reader/writer will be transmitted in the following format:

1. Start of Transmission (SOT).
2. N data bytes: N*(1 logic “0” start bit + 8 data bits + 1 logic “1” stop bit + 1 EGT(1) bit) N≥1.
3. (Optional) Two CRC bytes in the same format as above (2).
4. End of Transmission (EOT).

Note: 1. The EGT (Extra Guard Time) bit transmitted from the IC to the reader/writer is a logic “1”.

Figure 3. Type B Frame Format – IC to Reader/Writer (N Data Bytes)



Type B SOT/EOT

The Start of Transmission and End of Transmission sequences for Type B operation are defined below:

Start of Transmission (reader/writer to IC):

1. No carrier modulation.
2. The carrier is modulated (logic “0”) for 10 or 11 bit times.
3. The carrier is not modulated (logic “1”) for 2 or 3 bit times.

End of Transmission (reader/writer to IC):

1. No carrier modulation (this is the stop bit or EGT bit of the last data/command byte).
2. The carrier is modulated (logic “0”) for 10 or 11 bit times.
3. The reader stops modulating the carrier (logic “1”).

Start of Transmission (IC to reader/writer):

1. The carrier is modulated with the subcarrier for 10 bit times.
2. The subcarrier is phase shifted 180°.
3. The subcarrier is modulated with the carrier for 10 bit times with no subcarrier phase change.
4. The subcarrier is phase shifted 180°.
5. The subcarrier is modulated with the carrier for 2 bit times with no subcarrier phase changes.

Note: There will be a 180° phase change of the subcarrier between the end of the SOT and the start bit “0” if the DATA_ENCODE option is set to BPSK-NRZ-L. There will be no phase change of the subcarrier between the end of the SOT and the start bit “0” if the DATA_ENCODE option is set to BPSK-Miller.

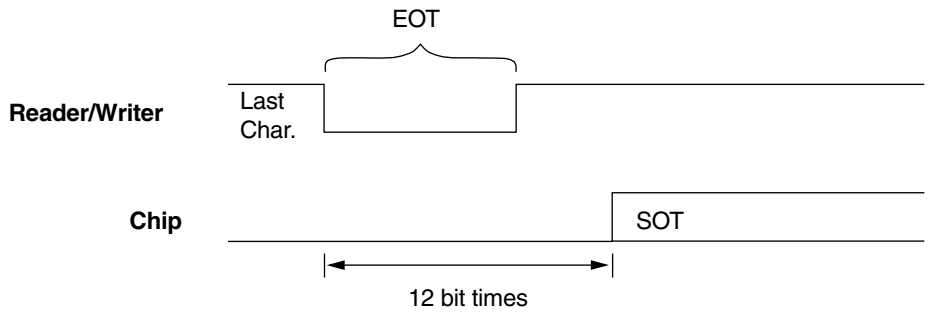
End of Transmission (IC to reader/writer):

1. A logic “0” (encoded in the format selected by the DATA_ENCODE option bit) is transmitted for 10 bit times.
2. A logic “1” (encoded in the format selected by the DATA_ENCODE option bit) is transmitted for 2 bit times.
3. The IC stops the subcarrier modulation.

Type B Timing

The IC will begin transmitting the SOT sequence (in response to a command or as an acknowledge) exactly 12 bit-times from the beginning of the reader/writer’s EOT.

Figure 4. Type B Frame Timing Restriction



CRC

Unless disabled by the CRC_OFF option bit, a 2-byte CRC code will end all frame transmissions (either from the IC or from the reader/writer). The CRC polynomial used in this device is identical to CRC_B as defined in ISO/IEC 14443-3: $x^{16} + x^{12} + x^5 + x^0$, or a hex polynomial of 1021. In this standard, the CRC register is initialized to 0xFFFF. When receiving information from the system, the IC computes the CRC on the incoming command, data and CRC bytes (start/stop bits, SOT, EOT and EGT are ignored). When the last bit of the CRC has been received, the value in the CRC register should be "0". When the IC transmits data, the CRC is computed based on the data bits. The CRC is transmitted as the final 2 bytes of the frame.

Pinout

Pin	Input/Output	Description
L1, L2	–	Coil Connection Pins
VDD	–	Power Supply 2.1V – 2.5V, also bypass cap
VSS	–	Ground
SCK	O	106 kHz Clock Output (SCL in two-wire mode)
CS	O	IC Select, Active-low
SO	O	Data Output (SDA – I/O for two-wire mode)
SI	I	Data Input (SPI only)

When configured to run in two-wire mode, SO becomes an open collector output, and an internal 15 kΩ (nominal) resistor is connected between SO and V_{DD}. In SPI and "simple I/O" mode all outputs are totem pole. There is a pull-down resistor on SI drawing 4 µA nominal at 2.4V. On power up, SO is configured as an input with a weak pull-up until the configuration memory is read to configure it per the application request.

Remaining pins on the serial memory (reset, write protect, addresses, etc.) must be tied high or low on the board containing the IC. In most cases with Atmel memories, these pins can also be left floating.

The IC includes a precision voltage reference to ensure that the IC operates only when the power-supply voltage on the device is above a required level of 1.8V – 2.0V. The on-board regulator will ensure that the V_{DD} voltage will be within the range of 2.1V – 2.5V.

The IC is capable of supporting up to 200 µA to the external device during communication. When communications have stopped (as during a write sequence), it can provide up to 2 mA of current to the external memory. Suitable bypass capacitance (0.01 µF) must be connected between the IC V_{DD} and GND pads for proper operation.

Ordering Information

Order Number	Version	External Bypass Cap	External IDD No Comm.	External IDD w/Comm.	Internal Current	Reset Voltage	V_{DD}
AT88RF001-01	EEPROM	10 nf	2 mA	200 µA	130 – 240 µA	1.8 – 2.0V	2.1 – 2.5V

Parametric Specifications

Parameter	Test Condition	Min	Typ	Max	Units
SPI Mode (CS, SO, SI, SCK)					
Input Low Voltage		–0.6		V_{DD} x 0.3	V
Input High Voltage		V_{DD} x 0.7		V_{DD} + 0.5	V
Output Low Voltage	$V_{DD} \geq 1.8V$ I_{OL} = 0.15 mA			0.2	V
Output High Voltage	$V_{DD} \geq 1.8V$ I_{OH} = –0.10 mA	V_{DD} –0.2			V
Two-wire Mode (SO, SCK)					
Input Low Voltage		–0.6		V_{DD} x 0.3	V
Input High Voltage		V_{DD} x 0.7		V_{DD} + 0.5	V
Output Low Voltage	$V_{DD} \geq 1.8V$ I_{OL} = 3 mA			0.4	V

Note: T = –40°C to 85°C, V_{DD} = 1.8V to 3.6V unless otherwise noted.

Mechanical Specifications

The IC is offered in a 16-lead SOIC package or as tested die on wafer. All I/O pads offer ESD protection at levels greater than 2 kV.

The input capacitance of the coil pins will vary from 7–13 pF, over process, temperature, voltage and frequency. The –01 and –02 versions of the IC do not include any additional capacitance.

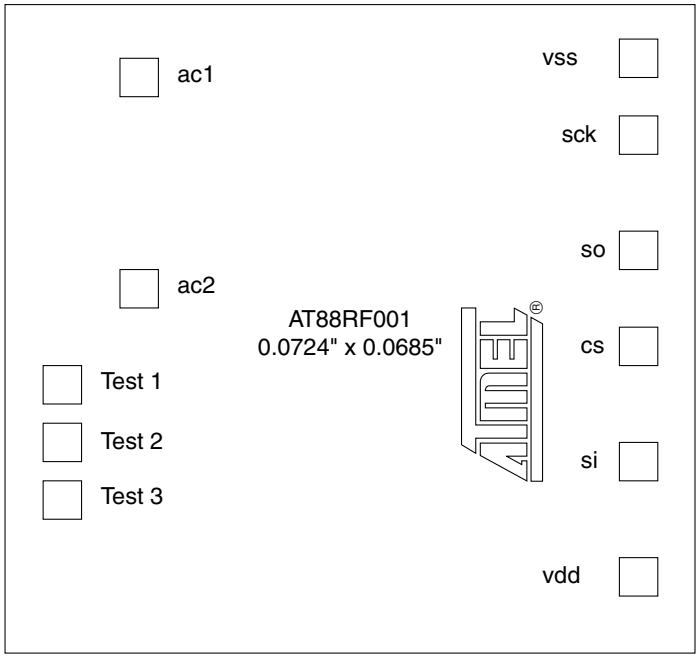
The layout of the die is shown on page 11. All pads are 90 µm x 90 µm with the exception of the three test pads, that are 80 µm x 80 µm. Coordinates for the pads are listed in the following table, measured to the nearest micron and referenced to the center of the die. The die size is the center-to-center distance on the wafer; actual die size after the saw operation will be smaller as a function of the saw kerf size and accuracy of cut.

Die Dimensions

Pad	X	Y
L1	–614.48 µm	710.32 µm
L2	–614.48 µm	77.52 µm
VSS (GND)	797.40 µm	752.72 µm
SCK	797.40 µm	575.64 µm
SO	797.40 µm	255.36 µm
SI	797.40 µm	–313.24 µm
VDD	797.40 µm	–635.36 µm
CS	797.40 µm	20.16 µm

Note: Test pads are for factory testing only.

Figure 5. AT88RF001 Die



Memory Map

The EEPROM is composed of 10 32-bit pages for a total of 320 bits. Pages 0–7 are the user pages, which include ID information and other user-defined bytes. Page 8 is the configuration page, which includes the lock and option bits. Page 9 is the password page.

	Byte 0	Byte 1	Byte 2	Byte 3
Page 0	First ID Byte	Second ID Byte	Third ID Byte	Fourth ID Byte
Page 1	Fifth ID Byte/User Data	Sixth ID Byte/User Data	Seventh ID Byte/User Data	Eighth ID Byte/User Data
Page 2	ID/User Data	ID/User Data	ID/User Data	ID/User Data
Page 3	ID/User Data	ID/User Data	ID/User Data	ID/User Data
Page 4	ID/User Data	ID/User Data	User Data	User Data
Page 5	User Data	User Data	User Data	User Data
Page 6	User Data	User Data	User Data	User Data
Page 7	User Data	User Data	User Data	User Data
Page 8	LOCK0…LOCK7	OPTIONS	OPTIONS	Reserved
Page 9	First Byte Password	Second Byte Password	Third Byte Password	Fourth Byte Password

Option Page

Bits are listed below in the order in which they must be sent to the IC when the Write Lock Byte or Write Config Bits command is sent to the IC.

When reading this page, all 32 bits are read in this order. This page cannot be written with a single 4-byte frame; the Write Lock Byte command is used for the first byte only, and the Write Config Bits command is used for the last three bytes. Changes to the options page do not take effect until the IC is reset by removing power or by sending an invalid command to the IC. The Default column reflects the default value that the options have upon shipment from Atmel.

Lock Byte

Name	Number of Bits	Default Value	Description
LOCK[0:7]	8	0	If “1”, locks the corresponding user page against further writes 10000000 Locks page 0 01000000 Locks page 1 ... and so on ...

Configuration Bits

Name	Number of Bits	Default Value	Description
PU_LEN[0:3]	4	0000	Number of ID bytes after first four. Total ID size range: 4–18 bytes. 0000 4 bytes . . . 1000 5 bytes 0111 18 bytes 0100 6 bytes
RANDOM	1	0	Frames (ID + 2-bit time listening window) between ID transmissions 0 Continuous frames 1 Random null frames, mean number = 16
PW_ON PW_EXT PW_LOCK	1 1 1	0 0 0	If “1”, password entry required before read/write cmds (password is page 9) If “1”, then the Send Begin command requires the correct password entry If “1”, locks the password page against further writes
CONFIG_LOCK	1	0	If “1”, locks the configuration page (but not LOCK[7:0]) against further writes
DATA_ENCODE	1	0	Transmit data using the following encoding: 0 BPSK-NRZ-L (ISO/IEC14443-2 Type B standard) 1 BPSK-Miller
CRC_OFF	1	0	If “1”, disables 2-byte CRC at the end of each frame transmission
SERIAL_MODE[0:1]	2	00	Determines the mode of the serial port 00 Two-wire (Master mode only, compatible with AT24Cxx) 01 SPI (Master only, mode 0) 10 SPI (Master only, mode 3) 11 Simple I/O mode (CLK, CS outputs; SI, SO inputs)
PAGE_SIZE[0:2]	3	000	Send/Get Page command byte count: 000 = 4 bytes, 001 = 8 bytes, 010 = 16 bytes, 011 = 32 bytes 100 = 64 bytes, 101 = 128 bytes, 11x = 256 bytes
RESERVED	8	–	These bits are for internal use. They return unpredictable values on a Read and cannot be written to.

Configuration Page Example

To write the configuration page, send the write configuration command and dummy AA byte, followed by the configuration bits and the two-byte CRC (if the optional CRC is enabled). In the following example, the configuration is being written to: PU_LEN = 8 ID bytes (0010), RANDOM = Continuous Frames (0), PW_ON = enabled (1), PW_EXT = enabled (1), CRC_Off = CRC enabled (0), SERIAL_MODE = SPI mode 0 (01), PAGE SIZE + 32 bytes (011). All other configuration bits are set to a default value of 0. The CRC_B bytes shown are correct for this data.

After sucessfully writing the configuration page, the IC will continuously transmit the contents of page 8. The changes in configuration will not take effect until the IC is reset by powering it down or by sending an invalid command to the IC.

Table 1. Configuration Page Example

Write Config	Dummy	Configuration			CRC_B	CRC_B
Command	Byte AA	Byte 1	Byte 2	Reserved	Byte 1	Byte 2
00010011	01010101	00100110	00001011	00000000	00100101	10011001
L S B						M S B

Pin connections to Atmel's two-wire and SPI serial EEPROMs are shown in Figure 6 and Figure 7.

Figure 6. Default Configuration – Two-wire Serial Memory

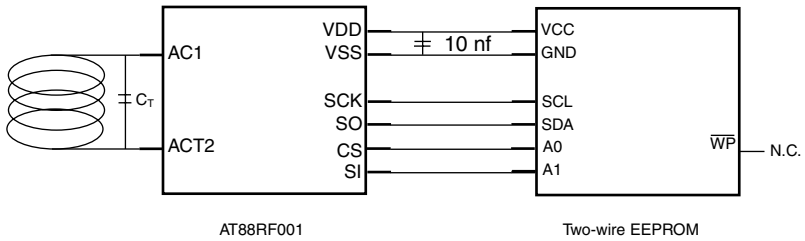
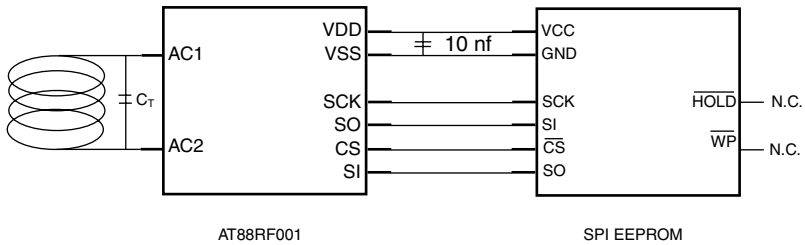
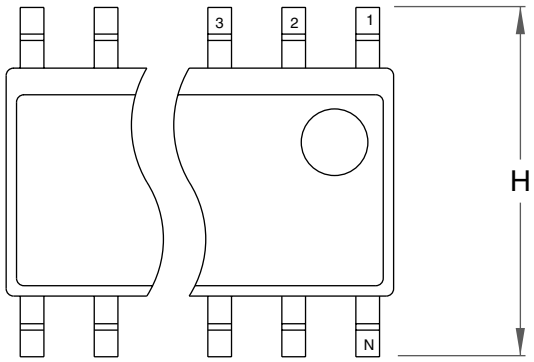


Figure 7. Configuration for SPI Serial Memory

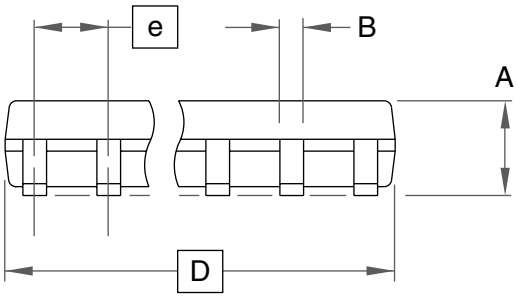


Package Drawing

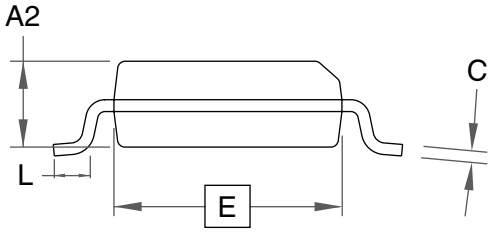
16S1 – SOIC



Top View



Side View



End View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
B	0.33	–	0.51	5
C	0.19	–	0.25	
D	9.80	–	10.00	2
E	3.80	–	4.00	3
e	1.27 BSC			
H	5.80	–	6.20	4
L	0.40	–	1.27	

Notes: 1. This drawing is for general information only; refer to JEDEC Drawing MS-012 for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed .15 mm (.006 in) per side.
3. Dimension E does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed .25 mm (.010 in) per side.
4. L is the length of terminal for soldering to a substrate.
5. The lead width B, as measured .36 mm (.014 in) or greater above the seating plane, shall not exceed a maximum value of .61 mm (.024 in).

10/15/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**16S1**, 16-lead, .150" Body, Plastic Gull Wing Small Outline (SOIC)	16S1	A

Sample Pinout[1][2]

Pin Name	Connection
Pin 1	ac2
Pin 2	Test 1
Pin 3	Test 2
Pin 4	Test 3
Pin 5	N/C
Pin 6	VDD
Pin 7	si
Pin 8	CS
Pin 9	SO
Pin 10	sck
Pin 11	GND (VSS)
Pin 12	N/C
Pin 13	N/C
Pin 14	N/C
Pin 15	N/C
Pin 16	ac1

Notes: 1. The on-IC tuning capacitor for samples is set at 10 pF.
2. The test pins (2, 3 and 4) are for factory testing only and should be left floating.

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