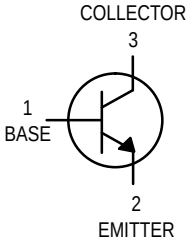
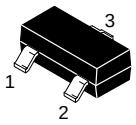
General Purpose Transistors
NPN Silicon

BCX70GLT1
BCX70JLT1
BCX70KLT1





CASE 318–08, STYLE 6
SOT–23 (TO–236AB)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	45	Vdc
Collector–Base Voltage	V_{CBO}	45	Vdc
Emitter–Base Voltage	V_{EBO}	5.0	Vdc
Collector Current — Continuous	I_C	200	mAdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR–5 Board(1) T_A = 25°C Derate above 25°C	P_D	225 1.8	mW mW/°C
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	556	°C/W
Total Device Dissipation Alumina Substrate,(2) T_A = 25°C Derate above 25°C	P_D	300 2.4	mW mW/°C
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	417	°C/W
Junction and Storage Temperature	T_J, T_{stg}	–55 to +150	°C

DEVICE MARKING

BCX70GLT1 = AG; BCX70JLT1 = AJ; BCX70KLT1 = AK

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Breakdown Voltage (I_C = 2.0 mAdc, I_E= 0)	$V_{(BR)CEO}$	45	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 1.0 μAdc, I_C = 0)	$V_{(BR)EBO}$	5.0	—	Vdc
Collector Cutoff Current (V_{CE} = 32 Vdc) (V_{CE} = 32 Vdc, T_A = 150°C)	I_{CES}	 — —	 20 20	 nAdc μAdc
Emitter Cutoff Current (V_{EB} = 4.0 Vdc, I_C = 0)	I_{EBO}	—	20	nAdc

1. FR–5 = 1.0 × 0.75 × 0.062 in.
2. Alumina = 0.4 × 0.3 × 0.024 in. 99.5% alumina.

Thermal Clad is a trademark of the Bergquist Company

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Continued)

Characteristic		Symbol	Min	Max	Unit
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			—
(I_C = 10 μAdc, V_{CE} = 5.0 Vdc)	BCX70G		—	—	
	BCX70J		40	—	
	BCX70K		100	—	
(I_C = 2.0 mAdc, V_{CE} = 5.0 Vdc)	BCX70G		120	220	
	BCX70J		250	460	
	BCX70K		380	630	
(I_C = 50 mAdc, V_{CE} = 1.0 Vdc)	BCX70G		60	—	
	BCX70J		90	—	
	BCX70K		100	—	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 50 mAdc, I_B = 1.25 mAdc)			—	0.55	
(I_C = 10 mAdc, I_B = 0.25 mAdc)			—	0.35	
Base–Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 50 mAdc, I_B = 1.25 mAdc)			0.7	1.05	
(I_C = 50 mAdc, I_B = 0.25 mAdc)			0.6	0.85	
Base–Emitter On Voltage		$V_{BE(on)}$	0.55	0.75	Vdc
(I_C = 2.0 mAdc, V_{CE} = 5.0 Vdc)					
SMALL–SIGNAL CHARACTERISTICS					
Current–Gain — Bandwidth Product		f_T	125	—	MHz
(I_C = 10 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)					
Output Capacitance		C_{obo}	—	4.5	pF
(V_{CB} = 10 Vdc, I_C = 0, f = 1.0 MHz)					
Small–Signal Current Gain		h_{fe}			—
(I_C = 2.0 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)	BCX70G		125	250	
	BCX70J		250	500	
	BCX70K		350	700	
Noise Figure		NF	—	6.0	dB
(I_C = 0.2 mAdc, V_{CE} = 5.0 Vdc, R_S = 2.0 kΩ, f = 1.0 kHz, BW = 200 Hz)					
SWITCHING CHARACTERISTICS					
Turn–On Time		t_{on}	—	150	ns
(I_C = 10 mAdc, I_{B1} = 1.0 mAdc)					
Turn–Off Time		t_{off}	—	800	ns
(I_{B2} = 1.0 mAdc, V_{BB} = 3.6 Vdc, R1 = R2 = 5.0 kΩ, R_L = 990Ω)					

EQUIVALENT SWITCHING TIME TEST CIRCUITS

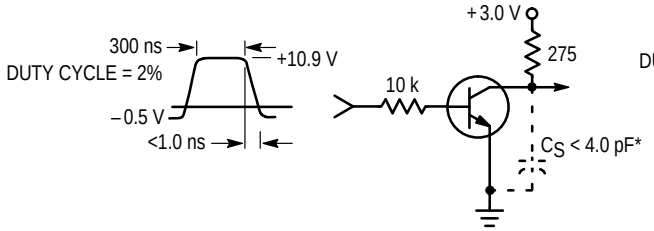


Figure 1. Turn–On Time

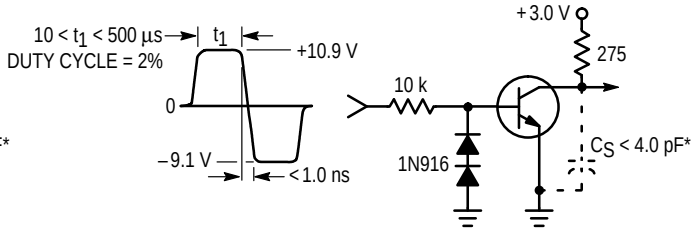


Figure 2. Turn–Off Time

*Total shunt capacitance of test jig and connectors

TYPICAL NOISE CHARACTERISTICS

(V_{CE} = 5.0 Vdc, T_A = 25°C)

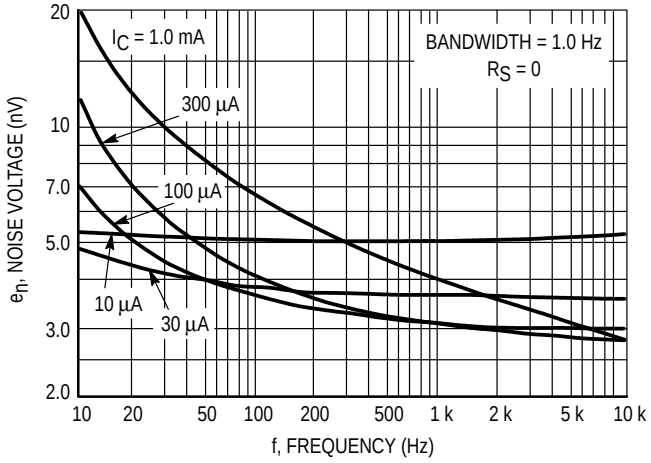


Figure 3. Noise Voltage

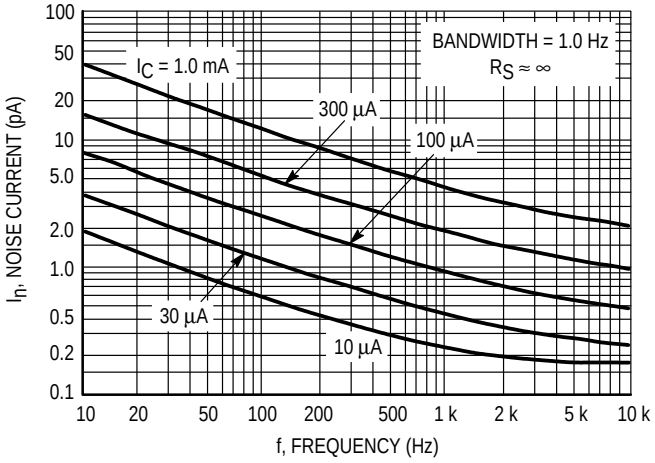


Figure 4. Noise Current

NOISE FIGURE CONTOURS

(V_{CE} = 5.0 Vdc, T_A = 25°C)

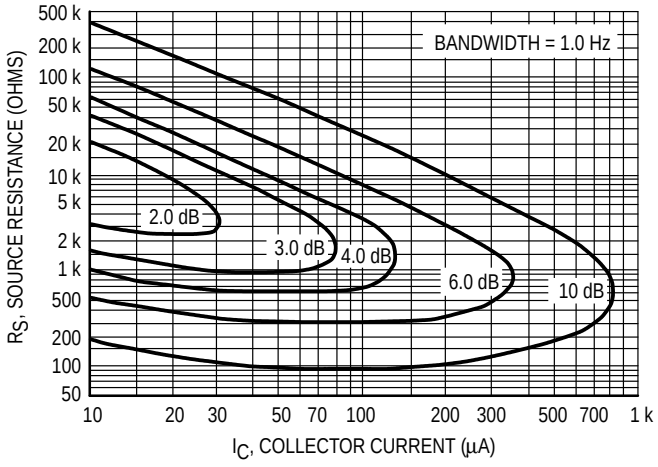


Figure 5. Narrow Band, 100 Hz

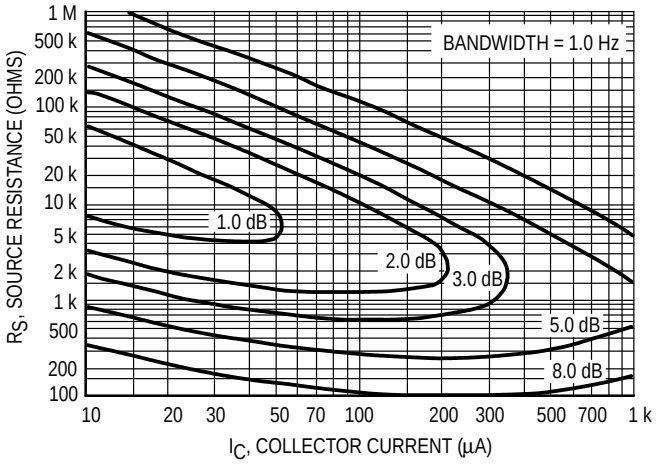


Figure 6. Narrow Band, 1.0 kHz

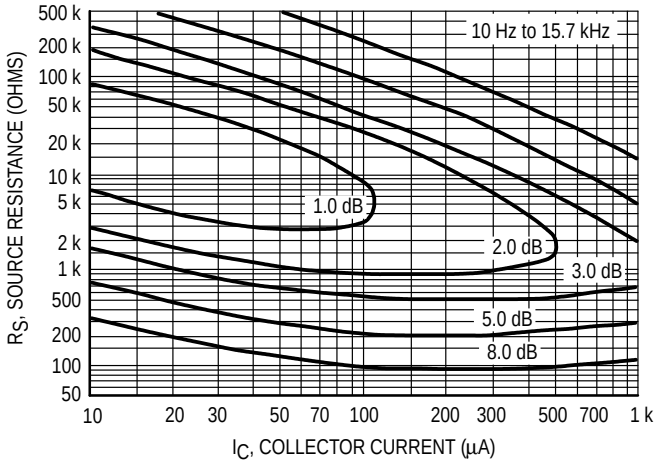


Figure 7. Wideband

Noise Figure is defined as:

$$NF = 20 \log_{10}\left(\frac{e_n^2 + 4KTR_S + I_n{}^2R_S{}^2}{4KTR_S}\right)^{1/2}$$

e_n = Noise Voltage of the Transistor referred to the input. (Figure 3)
I_n = Noise Current of the Transistor referred to the input. (Figure 4)
K = Boltzman's Constant (1.38 x 10^{-23} j/°K)
T = Temperature of the Source Resistance (°K)
R_S = Source Resistance (Ohms)

TYPICAL STATIC CHARACTERISTICS

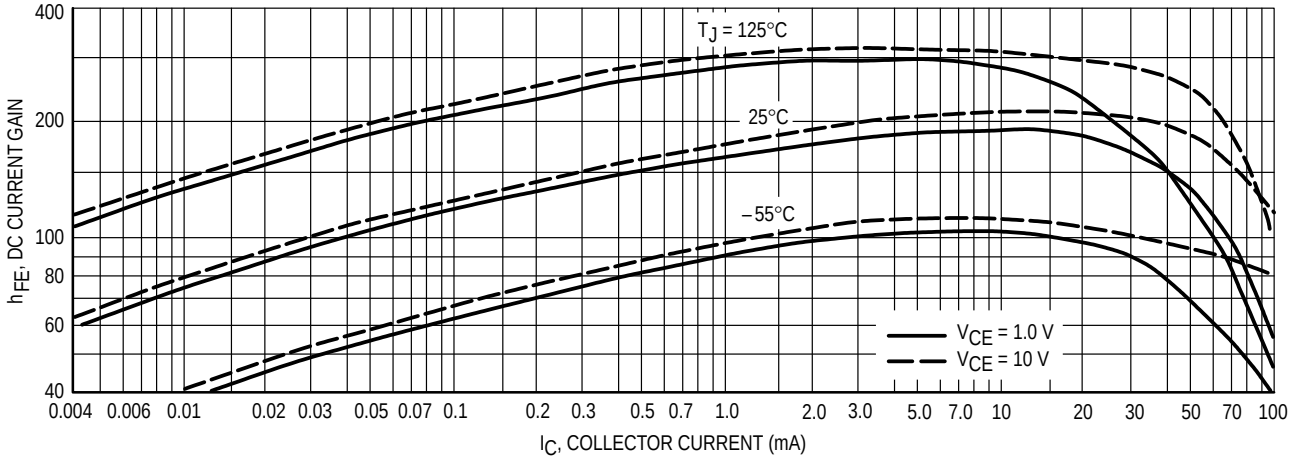


Figure 8. DC Current Gain

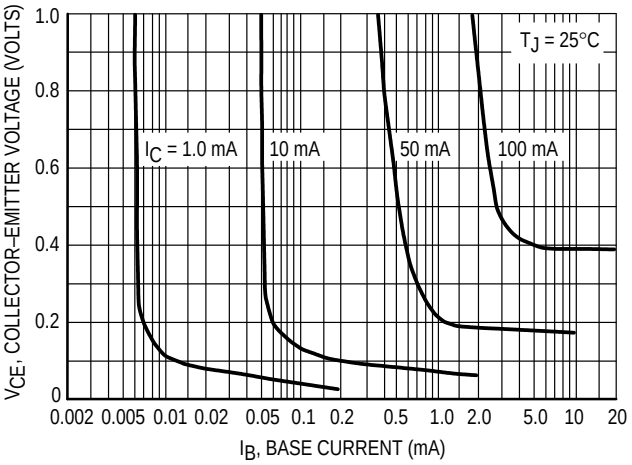


Figure 9. Collector Saturation Region

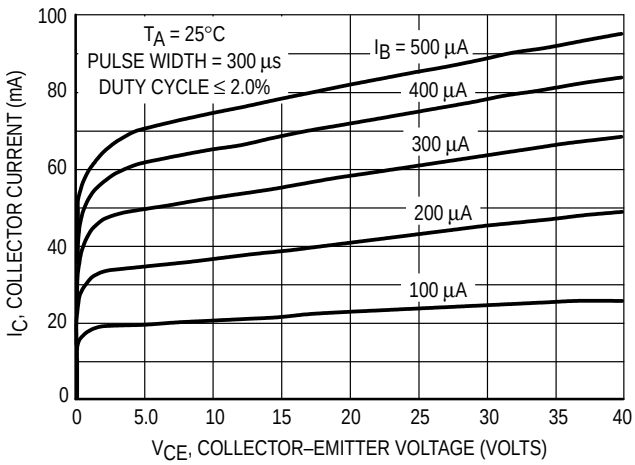


Figure 10. Collector Characteristics

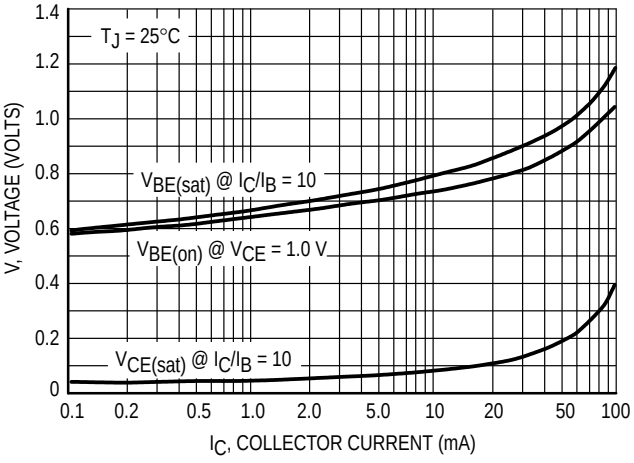


Figure 11. “On” Voltages

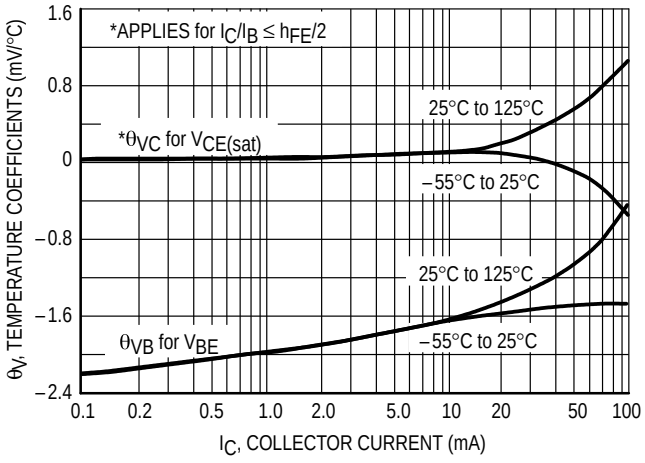


Figure 12. Temperature Coefficients

TYPICAL DYNAMIC CHARACTERISTICS

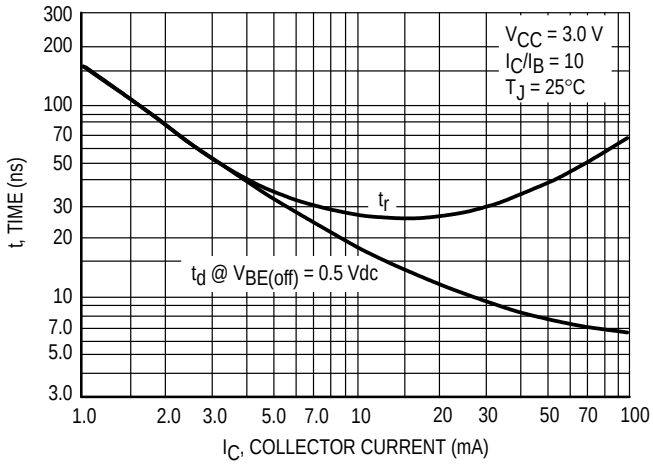


Figure 13. Turn–On Time

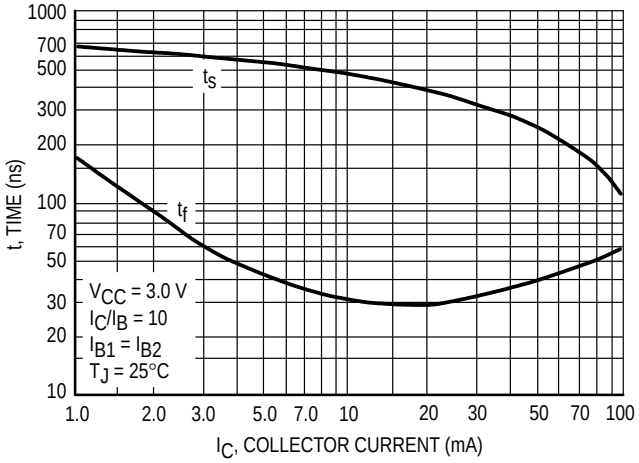


Figure 14. Turn–Off Time

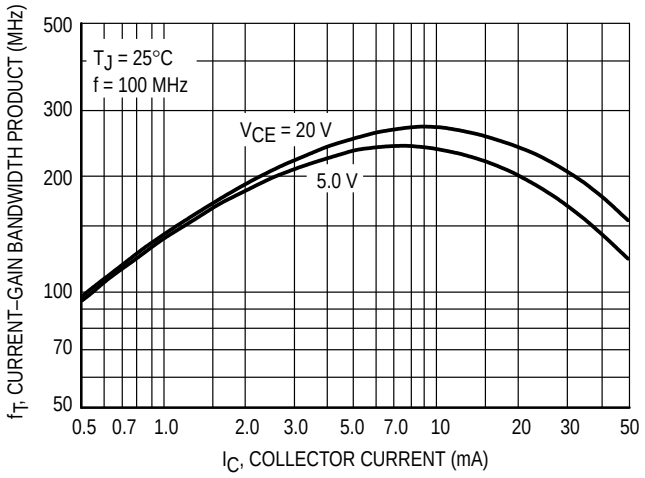


Figure 15. Current–Gain — Bandwidth Product

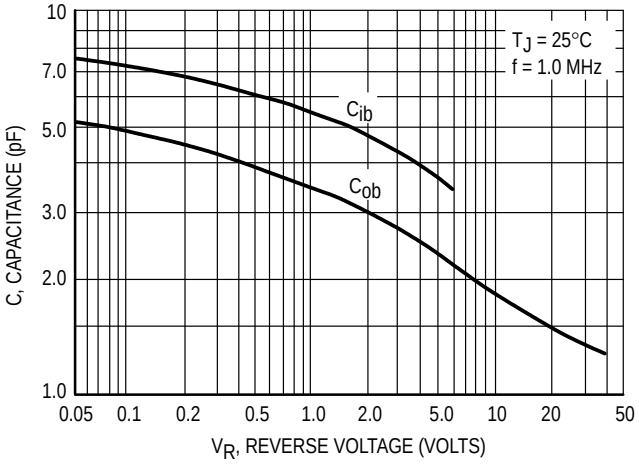


Figure 16. Capacitance

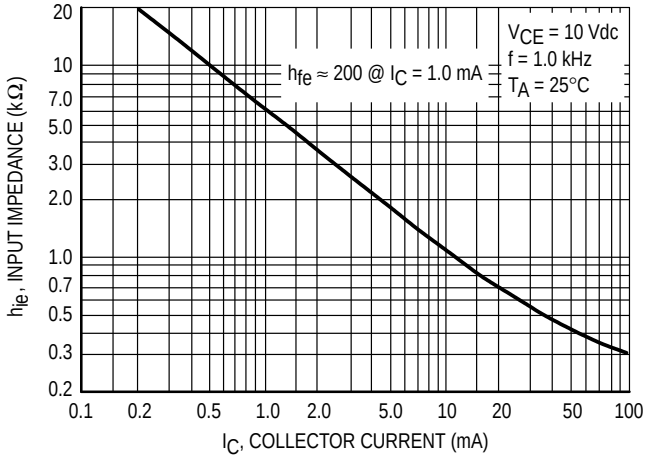


Figure 17. Input Impedance

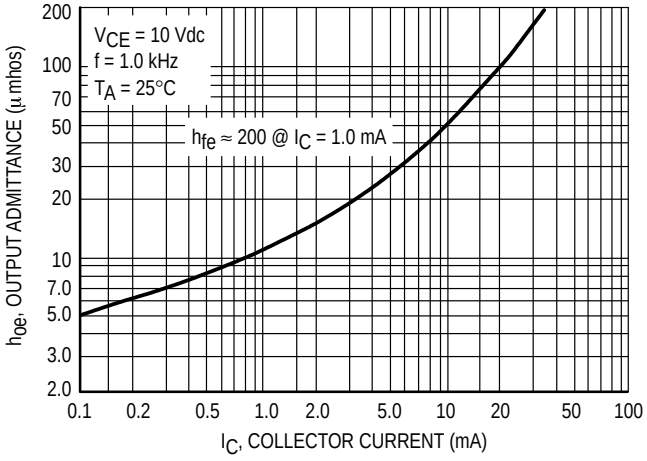


Figure 18. Output Admittance

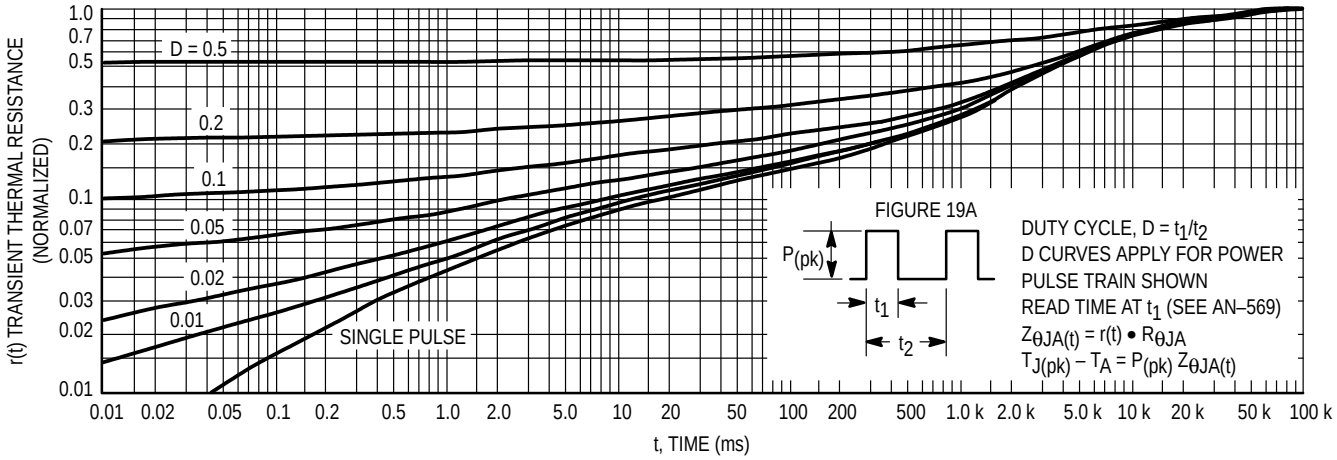


Figure 19. Thermal Response

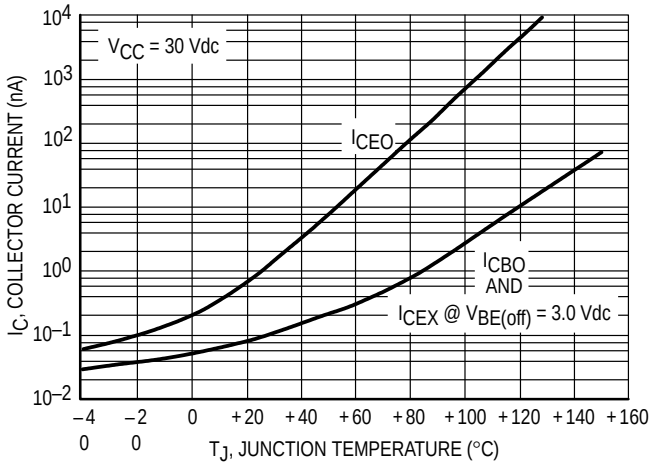


Figure 19A.

DESIGN NOTE: USE OF THERMAL RESPONSE DATA

A train of periodical power pulses can be represented by the model as shown in Figure 19A. Using the model and the device thermal response the normalized effective transient thermal resistance of Figure 19 was calculated for various duty cycles.

To find $Z_{\theta JA(t)}$, multiply the value obtained from Figure 19 by the steady state value $R_{\theta JA}$.

Example:

The MPS3904 is dissipating 2.0 watts peak under the following conditions:

t_1 = 1.0 ms, t_2 = 5.0 ms. (D = 0.2)

Using Figure 19 at a pulse width of 1.0 ms and D = 0.2, the reading of r(t) is 0.22.

The peak rise in junction temperature is therefore

$\Delta T = r(t) \times P_{(pk)} \times R_{\theta JA} = 0.22 \times 2.0 \times 200 = 88°C$.

For more information, see AN–569.

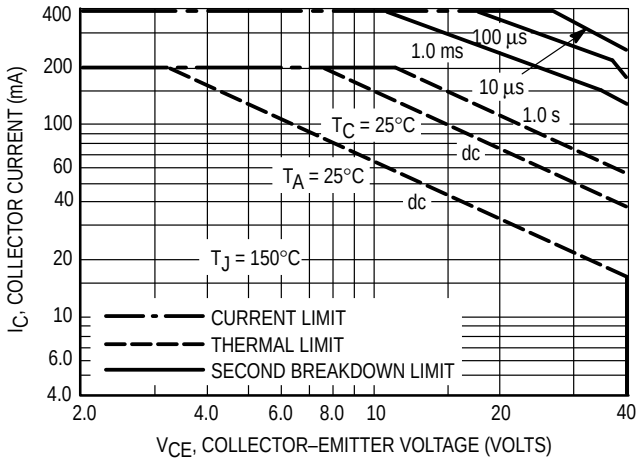


Figure 20.

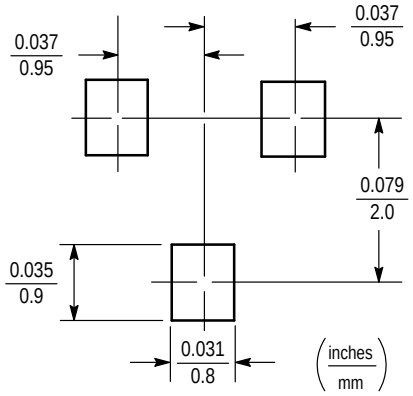
The safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation. Collector load lines for specific circuits must fall below the limits indicated by the applicable curve.

The data of Figure 20 is based upon $T_{J(pk)}$ = 150°C; T_C or T_A is variable depending upon conditions. Pulse curves are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 19. At high case or ambient temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

INFORMATION FOR USING THE SOT–23 SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



SOT–23

SOT–23 POWER DISSIPATION

The power dissipation of the SOT–23 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A. Using the values provided on the data sheet for the SOT–23 package, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 225 milliwatts.

$$P_D = \frac{150°C - 25°C}{556°C/W} = 225 \text{ milliwatts}$$

The 556°C/W for the SOT–23 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 225 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT–23 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

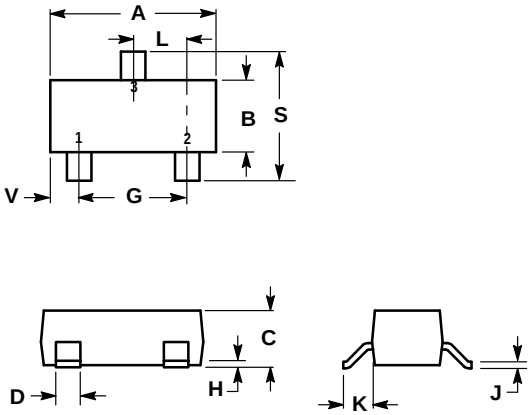
SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0180	0.0236	0.45	0.60
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.0984	2.10	2.50
V	0.0177	0.0236	0.45	0.60

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

CASE 318–08
ISSUE AE
SOT–23 (TO–236AB)

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