16 Bits Constant Current LED Driver

BD7851FP

General Description

BD7851FP is constant current LED driver which incorporates built-in 16 bits shift register and latch circuit.
A single external resistor can set the output current value of the constant current up to a maximum of 50mA.

Features

- The Constant Current Output
- Output line: 16 Bits
- Output type: Open Collector
- Cascade connection is possible

Applications

For AV equipment such as audio stereo sets, videos and TV sets, PCs, microcontroller-based mounted equipment.

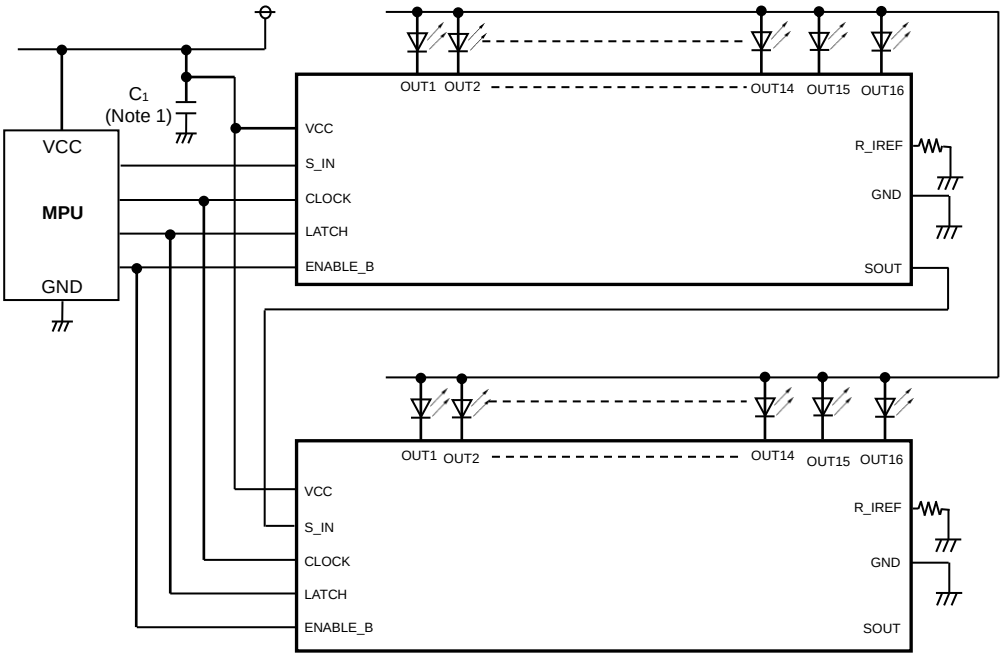
Key Specifications

- Power Supply Voltage Range: 4.5V to 5.5V
- Output Current: 50mA
- Frequency CLOCK: 10MHz(Max)
- Quiescent Current: 0.7mA(Typ)
- Operating Temperature Range: -30°C to +85°C

Package W(Typ) x D(Typ) x H(Max)

HSOP25
13.60mm x 7.80mm x 2.11mm

Typical Application Circuit

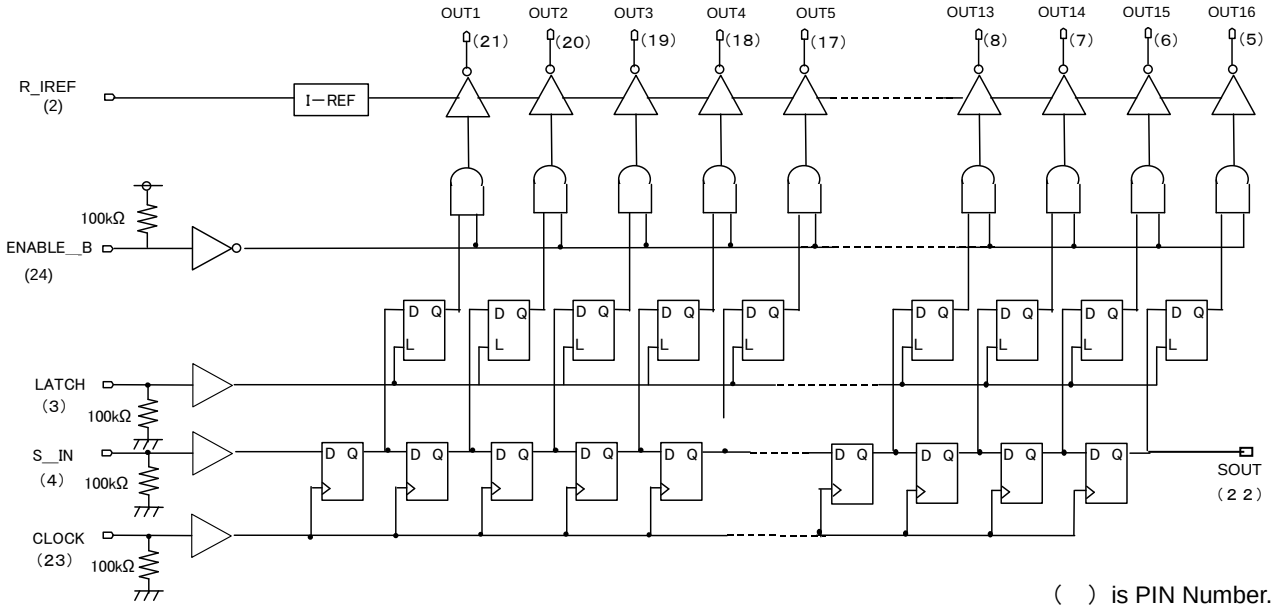


(Note 1) C_1 must be placed as close to the VCC terminal as possible.

Pin Descriptions

Pin No.	Pin Name	Function
1	GND	Ground
2	R_IREF	Constant current output current setting
3	LATCH	Latch signal input
4	S_IN	Serial data input
5 to 15	OUT16 to OUT6	Constant current output
16	P_GND	Ground for driver
17 to 21	OUT5 to OUT1	Constant current output
22	SOUT	Serial data output
23	CLOCK	Clock input
24	ENABLE_B	ENABLE_B signal input
25	VCC	VCC

Block Diagram



( ) is PIN Number.

(Note) OUTn is constant current output.

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limit	Unit
Power Supply Voltage	V_{CC}	0 to +7.0	V
Power Dissipation 1	Pd	1.45 (Note 1)	W
Input Voltage	V_{IN}	-0.3 to V_{CC}+0.3	V
Output Voltage (5pin to 15pin, 17pin to 21pin)	V_{OUT}	0 to +10	V
Operating Temperature	Topr	-30 to +85	°C
Storage Temperature	Tstg	-55 to +150	°C

(Note 1) Reduced by -11.6mW/°C over 25°C

Caution: An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

Electrical Characteristics

(Unless otherwise noted, Ta=25°C, V_{CC}=5.0V Test Circuit 1)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Power Supply Voltage	V_{CC}	4.5	-	5.5	V	
Input High-level Voltage	V_{IH}	0.8 x V_{CC}	-	-	V	
Input low-level Voltage	V_{IL}	-	-	0.2 x V_{CC}	V	
Output High-level Voltage	V_{OH}	V_{CC} - 0.5	-	-	V	I_{OL}=1mA
Output Low-level Voltage	V_{OL}	-	-	0.5	V	I_{OH}=-1mA
Current Consumption	I_{CC}	-	0.7	1.0	mA	R=13kΩ OUT1 to OUT16:OFF
		-	1.8	3.0	mA	R=1.3kΩ OUT1 to OUT16:OFF
		-	4.0	6.5	mA	R=13kΩ OUT1 to OUT16:ON
		-	30	40	mA	R=1.3kΩ OUT1 to OUT16:ON
Constant Current Output Current (including the equation between each bit)	Iolc1	48	55	62	mA	V_{OUT}=2.0V, R=1.3kΩ
	Iolc2	5.0	5.9	6.8	mA	V_{OUT}=2.0V, R=13kΩ
Equation between each bit of Constant Current Output Current	Δiolc	-	±1	±6	%	V_{OUTn}=2.0V, R=1.3kΩ (1bit : ON)
Change Rate of Constant Current Output Current for Output Voltage	IΔV_{CC}	-	±1	±6	%/V	V_{OUT}=2.0V to 3.0V, R=1.3kΩ
Output Leak Current	I_{OH}	-	0.01	0.8	μA	V_{OUT}=10V

Timing Characteristics

(Unless otherwise specified, V_{CC}=5V, Ta=25°C Test Circuit 2)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Frequency CLOCK	fclk	-	-	10	MHz	
Pulse Width CLOCK	t_{wh}	20	50	-	ns	CLOCK
Pulse Width LATCH	t_{wh}	40	50	-	ns	LATCH
Pulse Width ENABLE_B	t_w	30	-	-	ns	ENABLE_B
Rise Time / Fall Time	t_r / t_f	-	30	100	ns	CLOCK
Setup Time	t_{SU}	30	50	-	ns	S_IN-CLOCK
		30	50	-		LATCH-CLOCK
Hold Time	t_h	30	50	-	ns	S_IN-CLOCK
		30	50	-		LATCH-CLOCK
Rise Time	t_r	-	300	-	ns	OUTn
		-	-	50		SOUT
Fall Time	t_f	-	300	-	ns	OUTn
		-	-	50		SOUT
Propagation	t_{pLH}	-	400	650	ns	CLK-SOUT, LATCH ENABLE_B-OUTn
	t_{pHL}	-	300	400		CLK-SOUT, LATCH ENABLE_B-OUTn

Operation Timing Waveforms

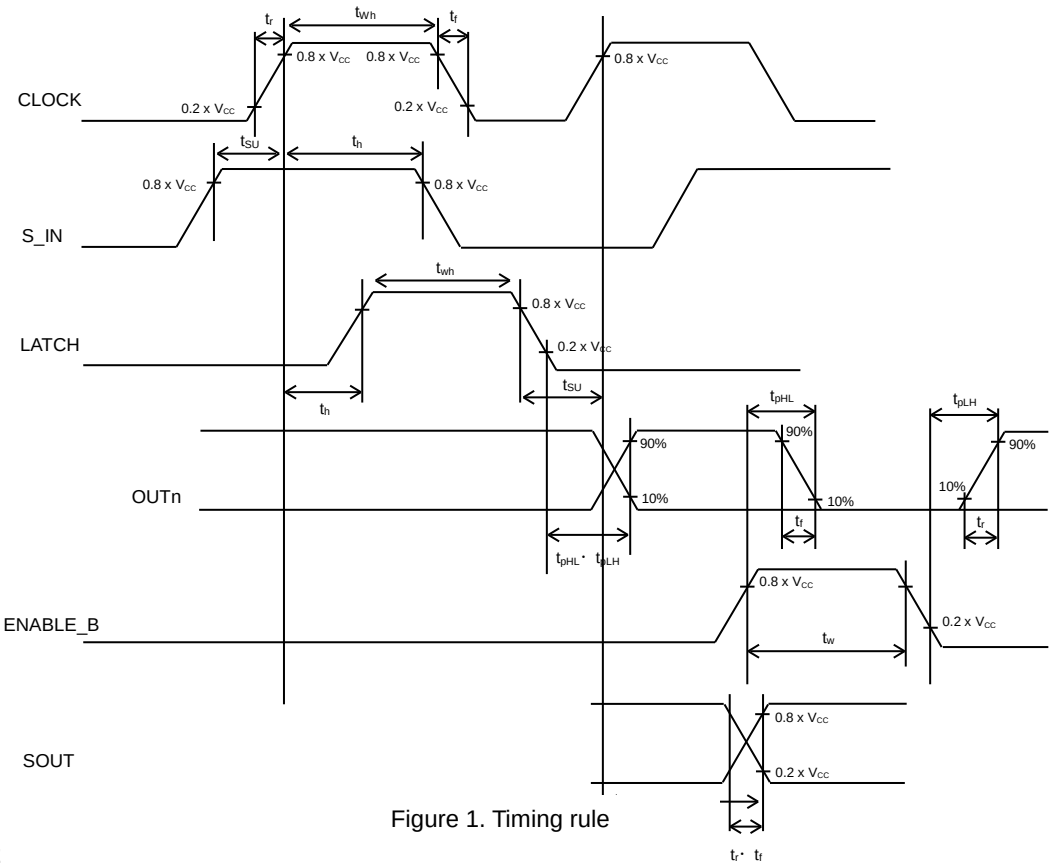


Figure 1. Timing rule

Timing Chart

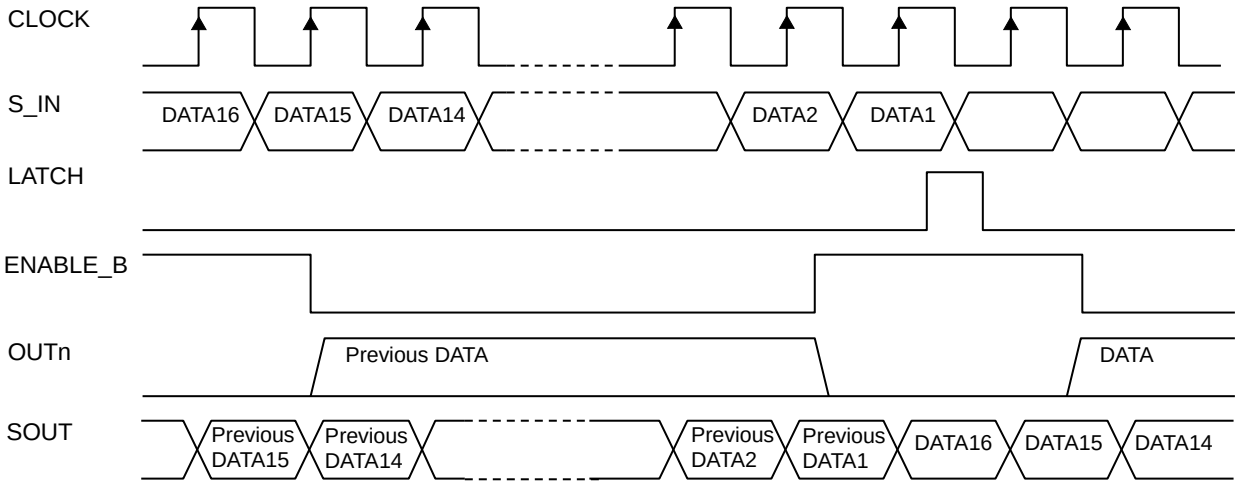
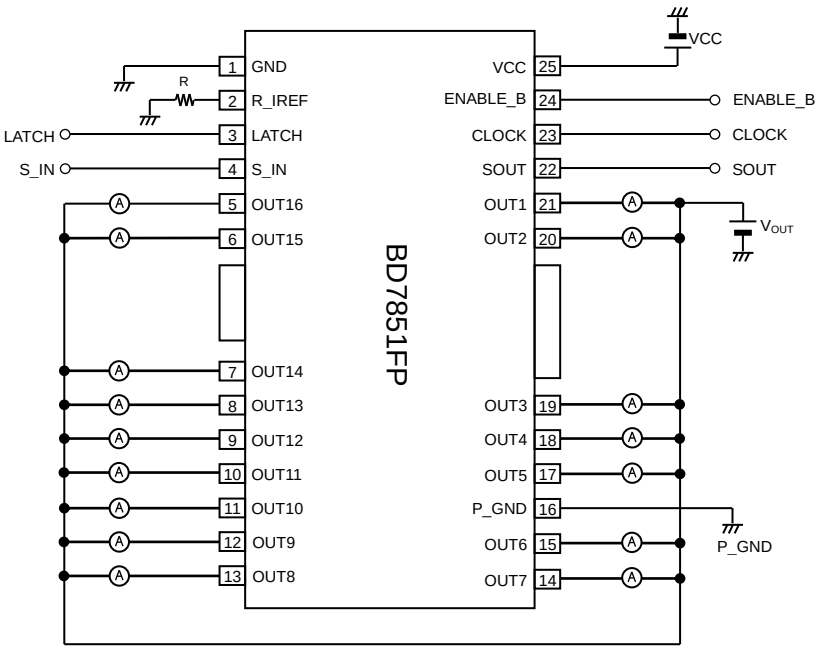


Figure 2. Timing chart

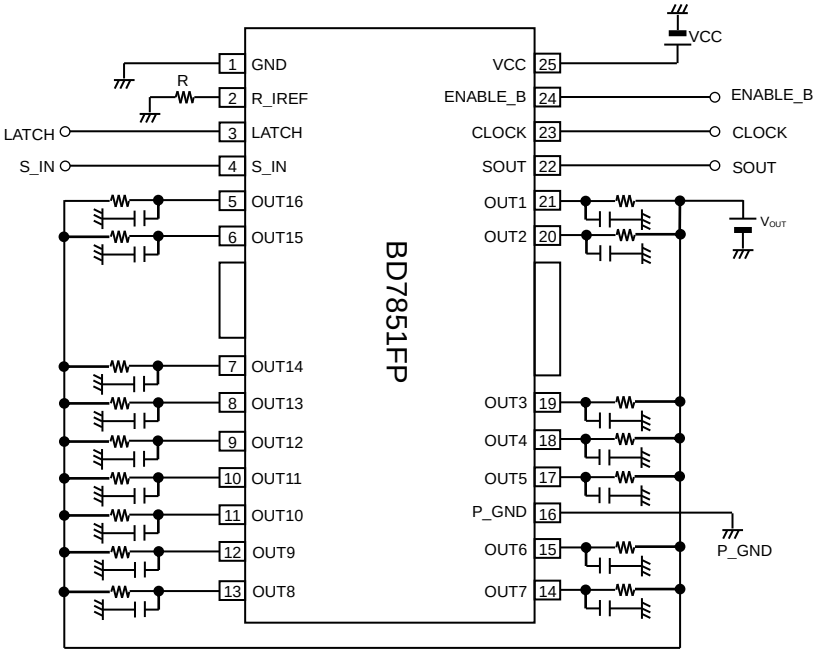
1. After the power is turned ON and the voltage is stabilized, LATCH should be activated after clocking 16 data bits into the S_IN terminal.
2. OUTn parallel output data of the shift register is set after the 16th clock by the LATCH.
3. The final stage data of the shift register is outputted to the SOUT by synchronizing with the rise time of the CLOCK.
4. Since the LATCH is a leveled latch, data is retained in the “L” section and renewed in the “H” section of the LATCH.
5. Data retained in the internal latch circuit is outputted when the ENABLE_B is in the “L” section. When the ENABLE_B is in the “H” section, data is fixed in the “H” section.

Application Information

1. Test Circuit 1

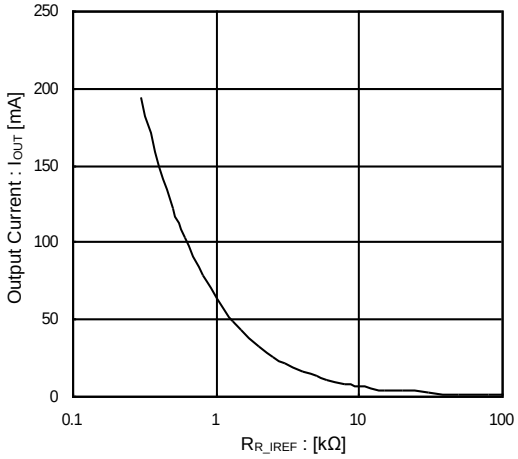


2. Test Circuit 2



(Note) R=51Ω (Note : R_{R_IREF}=1.3kΩ) , C=15pF

3. Constant Current of Output Current



[Condition]
V_{CC}=5.0V, V_{OUT}=5.0V, Ta=25°C

The Constant current of output current is determined by the external resistor. (Between 2pin and GND)

(Note) This is a data for the standard sample, not guaranteed the characteristic.

Figure 3. Constant Current of Output Current

4. Explanation of operation

(1) Setting of current value of constant-current output
Specify the constant-current value according to external resistor. Connect the external resistor between 2PIN and GND.
Specify the external resistor value based on the constant-current output current characteristic shown in Figure 2.
(Note) If the state between 2PIN and GND is open, the output current does not flow.
If GND is short-circuited, an excessive current flows.

(2) Explanation of input terminal

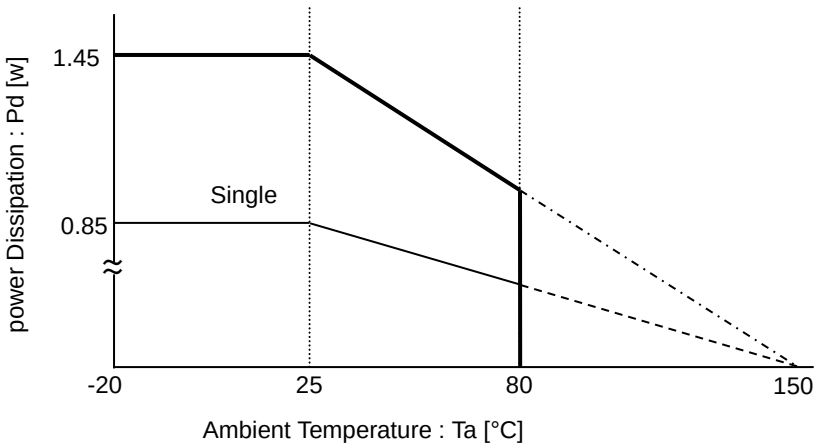
S_IN ・・・・・・ Serial data input terminal of shift register.
CLOCK ・・・・ CLOCK input terminal. The shift register shifts a data at this leading edge.
LATCH ・・・・ LATCH signal input terminal. Level latch. A data of the shift register is updated at the High level and the data is held at the Low level.
ENABLE_B ・・ OUTPUT ENABLE terminal. A data held in LATCH is output at the Low level. The output is turned OFF forcibly at the High level.

(3) Explanation of output terminal

OUTn ・・・・・・ Constant-current output terminal. Open collector method.
SOUT ・・・・・・ Serial data output terminal.

(4) TSD (Thermal Shutdown) function
When the IC temperature rise considerably, the high temperature is detected. If the detected temperature is higher a specified level, the constant-current output is turned OFF forcibly.

Power Dissipation



(Note) A glass epoxy board 70 mm x 70 mm x 1.6 mm is mounted.

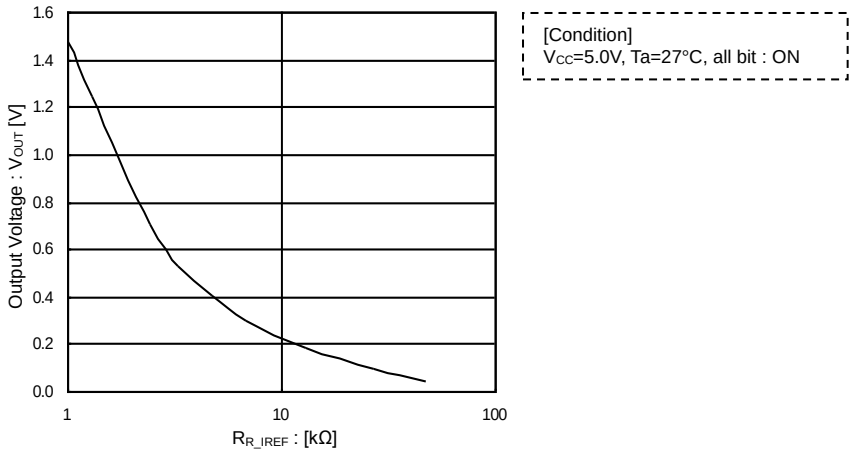
Heat resistance varies depending on the mount state. This IC achieves low heat resistance by heat radiation through heat radiation PIN. So, be sure to solder the heat radiation PIN to a low heat impedance pattern.

The temperature around the heat PIN rises. Select any suitable printed board material taking the temperature characteristic into consideration.

Allowable dissipation Pd

If this IC is used exceeding the allowable dissipation, the current capacity may decrease and the IC performance may deteriorate due to the chip temperature rise. Please be sure to use this IC within the allowable dissipation.

R_{R_IREF}-V_{OUT}



(Note) If V_{OUT} voltage is made lower, the current consumption I_{CC} will increase, please consider V_{OUT} value based on the graph above

Figure 4. R_IREF - V_{OUT}

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

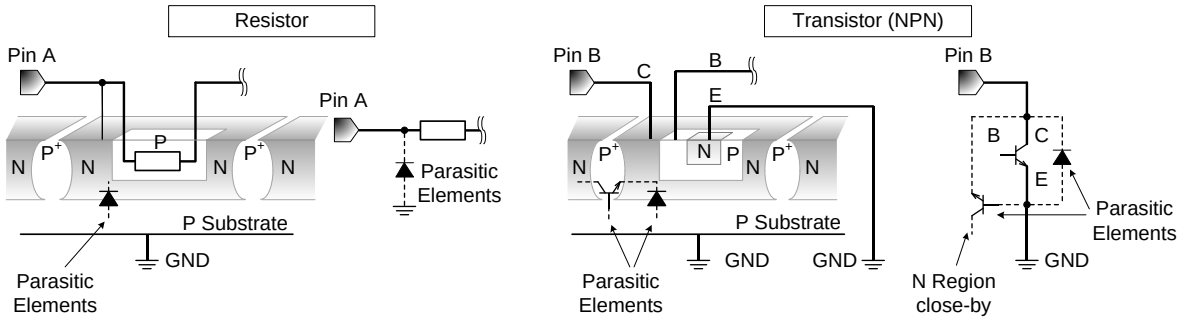
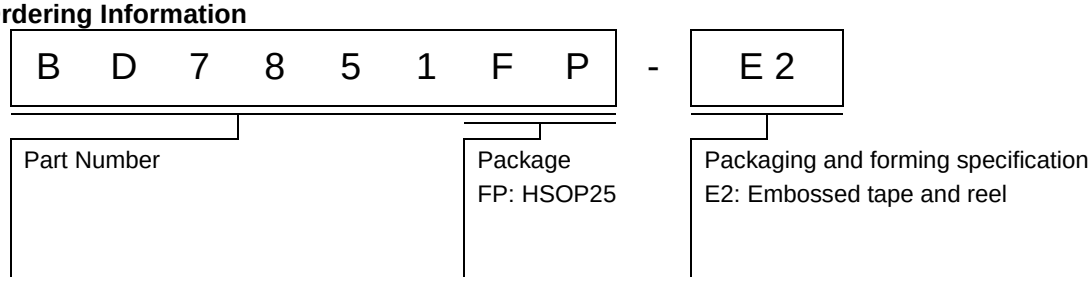
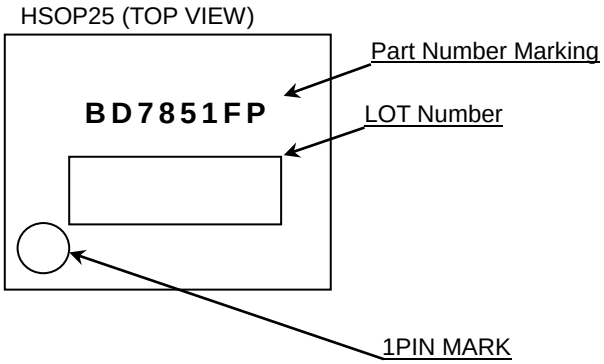


Figure 5. Example of monolithic IC structure

Ordering Information

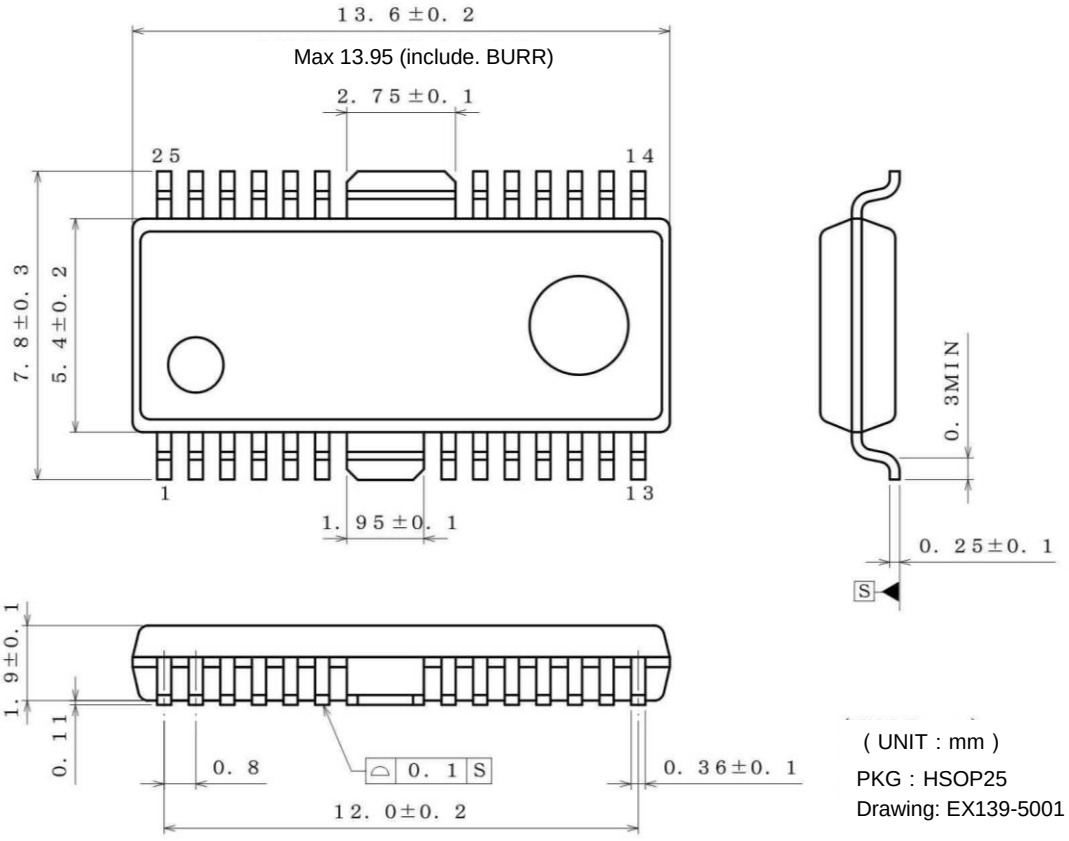


Marking Diagram



Physical Dimension, Tape and Reel Information

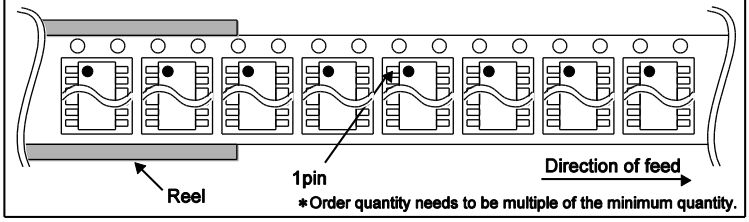
Package Name	HSOP25



(UNIT : mm)
PKG : HSOP25
Drawing: EX139-5001

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Revision	Changes
09.Feb.2016	001	New Release

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JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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