

# NPN Plastic Silicon Power Transistor

... designed for low power audio amplifier and low-current, high speed switching applications.

• High Collector–Emitter Sustaining Voltage —

 $V_{CEO(sus)} = 100 \text{ Vdc (Min)}$ 

• High DC Current Gain @ I<sub>C</sub> = 200 mAdc

 $h_{FE} = 40-250$ 

• Low Collector–Emitter Saturation Voltage —

 $V_{CE(sat)} = 0.5 \text{ Vdc (Max)} @ I_C = 500 \text{ mAdc}$ 

• High Current Gain — Bandwidth Product —

 $f_T = 40 \text{ MHz (Min)} @ I_C = 100 \text{ mAdc})$ 

### \*MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector–Emitter Voltage	V <sub>CEO</sub>	100	Vdc
Collector-Base Voltage	V <sub>CB</sub>	100	Vdc
Emitter–Base Voltage	V <sub>EBO</sub>	6.0	Vdc
Collector Current — Continuous — Peak	Ic	4.0 8.0	Adc
Base Current	Ι <sub>Β</sub>	1.0	Adc
Total Power Dissipation @ T <sub>C</sub> = 25°C Derate above 25°C	P <sub>D</sub>	15 0.12	Watts W/°C
Operating and Storage Junction Temperature Range	T <sub>J</sub> ,T <sub>stg</sub>	-65 to +150	°C

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.34	°C/W

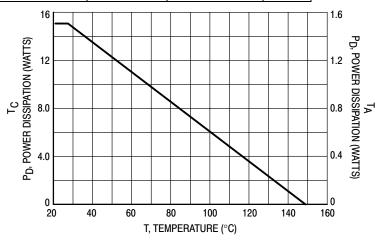


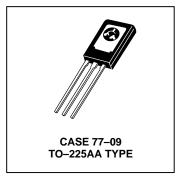
Figure 1. Power Derating

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

### **BD791**

**ON Semiconductor Preferred Device** 

4 AMPERE
POWER TRANSISTOR
SILICON
100 VOLTS
15 WATTS

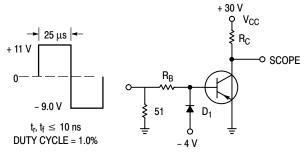


### \*ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
DFF CHARACTERISTICS			•	1
Collector–Emitter Sustaining Voltage (1)	V <sub>CEO(sus)</sub>			Vdc
$(I_C = 10 \text{ mAdc}, I_B = 0)$		100	_	
Collector Cutoff Current	I <sub>CEO</sub>			μAdc
$(V_{CE} = 50 \text{ Vdc}, I_B = 0)$		_	100	
Collector Cutoff Current	I <sub>CEX</sub>			
$(V_{CE} = 100 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ Vdc})$		—	1.0	μAdc
$(V_{CE} = 50 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ Vdc}, T_{C} = 125^{\circ}\text{C})$		_	0.1	mAdc
Emitter Cutoff Current (V <sub>EB</sub> = 6.0 Vdc, I <sub>C</sub> = 0)	I <sub>EBO</sub>	_	1.0	μAdc
ON CHARACTERISTICS (1)				
DC Current Gain	h <sub>FE</sub>			_
$(I_C = 200 \text{ mAdc}, V_{CE} = 3.0 \text{ Vdc})$		40	250	
$(I_C = 1.0 \text{ Adc}, V_{CE} = 3.0 \text{ Vdc})$		20	_	
$(I_C = 2.0 \text{ Adc}, V_{CE} = 3.0 \text{ Vdc})$		10		
$(I_C = 4.0 \text{ Adc}, V_{CE} = 3.0 \text{ Vdc})$		5.0	_	
Collector Emitter Saturation Voltage	V <sub>CE(sat)</sub>			Vdc
$(I_C = 500 \text{ mAdc}, I_B = 50 \text{ mAdc})$	2 = (53.7)	_	0.5	
$(I_C = 1.0 \text{ Adc}, I_B = 100 \text{ mAdc})$		_	1.0	
$(I_C = 2.0 \text{ Adc}, I_B = 200 \text{ mAdc})$		_	2.5	
(I <sub>C</sub> = 4.0 Adc, I <sub>B</sub> = 800 mAdc)		_	3.0	
Base–Emitter Saturation Voltage (I <sub>C</sub> = 2.0 Adc, I <sub>B</sub> = 200 mAdc)	V <sub>BE(sat)</sub>	_	1.8	Vdc
Base–Emitter On Voltage (I <sub>C</sub> = 200 mAdc, V <sub>CE</sub> = 3.0 Vdc)	V <sub>BE(on)</sub>		1.5	Vdc
DYNAMIC CHARACTERISTICS	, , ,		1	I
Current-Gain — Bandwidth Product	f <sub>T</sub>	40	_	MHz
$(I_C = 100 \text{ mAdc}, V_{CE} = 10 \text{ Vdc}, f = 10 \text{ MHz})$	, ,			
Output Capacitance	C <sub>ob</sub>			pF
$(V_{CB} = 10 \text{ Vdc}, I_C = 0, f = 0.1 \text{ MHz})$		_	50	
Small–Signal Current Gain	h <sub>fe</sub>	10	_	_
$(I_C = 200 \text{ mAdc}, V_{CE} = 10 \text{ Vdc}, f = 1.0 \text{ kHz})$				

<sup>\*</sup>Indicates JEDEC Registered Data.

<sup>(1)</sup> Pulse Test: Pulse Width  $\leq 300 \, \mu s$ , Duty Cycle  $\leq 2.0\%$ .



 $R_B$  and  $R_C$  varied to obtain desired current levels  $D_1$  must be fast recovery type, eg  $$\rm MBR340$  used above  $I_B\approx 100$  ma  $\rm MSD6100$  used below  $I_B\approx 100$  ma for PNP test circuit, reverse all polarities.

Figure 2. Switching Time Test Circuit

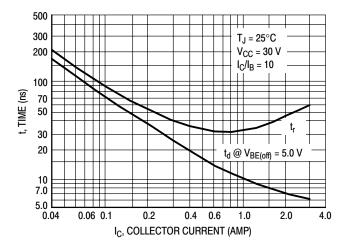


Figure 3. Turn-On Time

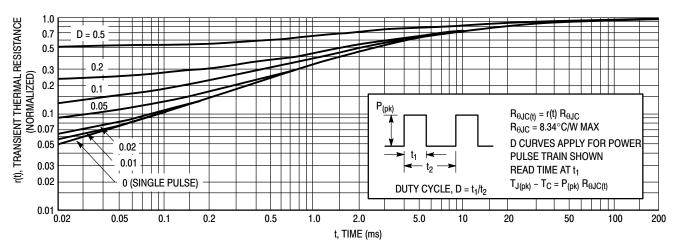


Figure 4. Thermal Response

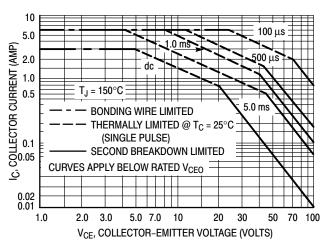


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_{J(pk)} = 150^{\circ}C$ :  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \le 150^{\circ}C$ ,  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

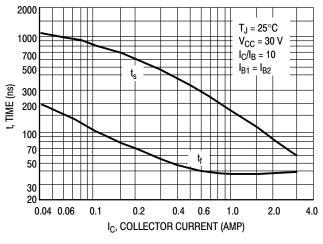


Figure 6. Turn-Off Time

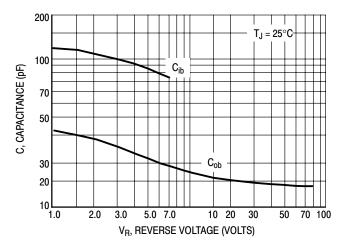
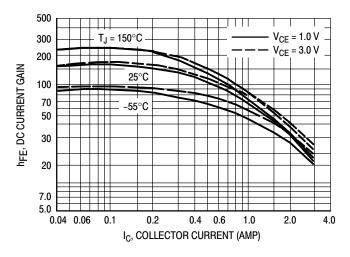


Figure 7. Capacitance



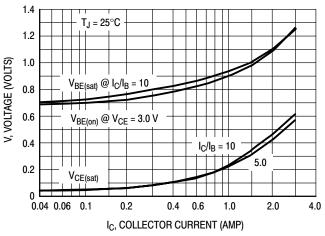
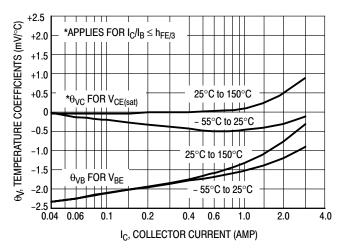


Figure 8. DC Current Gain

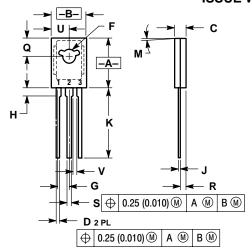
Figure 9. "On" Voltage



**Figure 10. Temperature Coefficient** 

### **PACKAGE DIMENSIONS**

### **CASE 77-09** TO-225AA TYPE **ISSUE W**



- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS		
DIM	MIN	MAX	MIN	MAX	
Α	0.425	0.435	10.80	11.04	
В	0.295	0.305	7.50	7.74	
С	0.095	0.105	2.42	2.66	
D	0.020	0.026	0.51	0.66	
F	0.115	0.130	2.93	3.30	
G	0.094 BSC		2.39 BSC		
Н	0.050	0.095	1.27	2.41	
J	0.015	0.025	0.39	0.63	
K	0.575	0.655	14.61	16.63	
M	5° TYP		5°	5° TYP	
Q	0.148	0.158	3.76	4.01	
R	0.045	0.065	1.15	1.65	
S	0.025	0.035	0.64	0.88	
U	0.145	0.155	3.69	3.93	
V	0.040		1.02		

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

## **Notes**

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JAPAN: ON Semiconductor, Japan Customer Focus Center

4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-0031

Phone: 81-3-5740-2700

Email: r14525@onsemi.com

ON Semiconductor Website: http://onsemi.com

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