DATA SHEET

BFR540
NPN 9 GHz wideband transistor

Product specification
Supersedes data of 1995 September

1999 Aug 23

Philips
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NPN 9 GHz wideband transistor — BFR540

FEATURES

- High power gain
- Low noise figure
- High transition frequency
- Gold metallization ensures excellent reliability.

DESCRIPTION

The BFR540 is an npn silicon planar epitaxial transistor, intended for applications in the RF frontend in wideband applications in the GHz range, such as analog and digital cellular telephones, cordless telephones (CT1, CT2, DECT, etc.), radar detectors, satellite TV tuners (SATV), MATV/CATV amplifiers and repeater amplifiers in fibre-optic systems.

The transistor is encapsulated in a plastic SOT23 envelope.

PINNING

PIN	DESCRIPTION
Code: N29	
1	base
2	emitter
3	collector

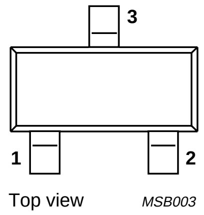


Fig.1 SOT23.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	–	20	V
V_{CES}	collector-emitter voltage	$R_{BE} = 0$	–	–	15	V
I_C	DC collector current		–	–	120	mA
P_{tot}	total power dissipation	up to $T_s = 70$ °C; note 1	–	–	500	mW
h_{FE}	DC current gain	$I_C = 40$ mA; $V_{CE} = 8$ V	60	120	250	
C_{re}	feedback capacitance	$I_C = i_c = 0$; $V_{CB} = 8$ V; f = 1 MHz	–	0.6	–	pF
f_T	transition frequency	$I_C = 40$ mA; $V_{CE} = 8$ V; f = 1 GHz	–	9	–	GHz
G_{UM}	maximum unilateral power gain	$I_C = 40$ mA; $V_{CE} = 8$ V; $T_{amb} = 25$ °C; f = 900 MHz	–	14	–	dB
		$I_C = 40$ mA; $V_{CE} = 8$ V; $T_{amb} = 25$ °C; f = 2 GHz	–	7	–	dB
$\|S_{21}\|^2$	insertion power gain	$I_C = 40$ mA; $V_{CE} = 8$ V; $T_{amb} = 25$ °C; f = 900 MHz	12	13	–	dB
F	noise figure	$\Gamma_s = \Gamma_{opt}$; $I_C = 10$ mA; $V_{CE} = 8$ V; $T_{amb} = 25$ °C; f = 900 MHz	–	1.3	1.8	dB
		$\Gamma_s = \Gamma_{opt}$; $I_C = 40$ mA; $V_{CE} = 8$ V; $T_{amb} = 25$ °C; f = 900 MHz	–	1.9	2.4	dB
		$\Gamma_s = \Gamma_{opt}$; $I_C = 10$ mA; $V_{CE} = 8$ V; $T_{amb} = 25$ °C; f = 2 GHz	–	2.1	–	dB

Note

1. T_s is the temperature at the soldering point of the collector tab.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	20	V
V_{CES}	collector-emitter voltage	$R_{BE} = 0$	–	15	V
V_{EBO}	emitter-base voltage	open collector	–	2.5	V
I_C	DC collector current		–	120	mA
P_{tot}	total power dissipation	up to T_s = 70 °C; note 1	–	500	mW
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	175	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}s}$	from junction to soldering point	see note 1	260 K/W

Note

1. T_s is the temperature at the soldering point of the collector tab.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector cut-off current	$I_E = 0$; V_{CB} = 8 V	–	–	50	nA
h_{FE}	DC current gain	I_C = 40 mA; V_{CE} = 8 V	60	120	250	
C_e	emitter capacitance	$I_C = i_c = 0$; V_{EB} = 0.5 V; f = 1 MHz	–	2	–	pF
C_c	collector capacitance	$I_E = i_e = 0$; V_{CB} = 8 V; f = 1 MHz	–	0.9	–	pF
C_{re}	feedback capacitance	$I_C = 0$; V_{CB} = 8 V; f = 1 MHz	–	0.6	–	pF
f_T	transition frequency	I_C = 40 mA; V_{CE} = 8 V; f = 1 GHz	–	9	–	GHz
G_{UM}	maximum unilateral power gain (note 1)	I_C = 40 mA; V_{CE} = 8 V; T_{amb} = 25 °C; f = 900 MHz	–	14	–	dB
		I_C = 40 mA; V_{CE} = 8 V; T_{amb} = 25 °C; f = 2 GHz	–	7	–	dB
$\|S_{21}\|^2$	insertion power gain	I_C = 40 mA; V_{CE} = 8 V; T_{amb} = 25 °C; f = 900 MHz	12	13	–	dB
F	noise figure	$\Gamma_s = \Gamma_{opt}$; I_C = 10 mA; V_{CE} = 8 V; T_{amb} = 25 °C; f = 900 MHz	–	1.3	1.8	dB
		$\Gamma_s = \Gamma_{opt}$; I_C = 40 mA; V_{CE} = 8 V; T_{amb} = 25 °C; f = 900 MHz	–	1.9	2.4	dB
		$\Gamma_s = \Gamma_{opt}$; I_C = 10 mA; V_{CE} = 8 V; T_{amb} = 25 °C; f = 2 GHz	–	2.1	–	dB
P_{L1}	output power at 1 dB gain compression	I_C = 40 mA; V_{CE} = 8 V; R_L = 50 Ω; T_{amb} = 25 °C; f = 900 MHz	–	21	–	dBm
ITO	third order intercept point	note 2	–	34	–	dBm
V_o	output voltage (note 3)	I_C = 40 mA; V_{CE} = 8 V; $Z_L = Z_S$ = 75 Ω; T_{amb} = 25 °C	–	550	–	mV

Notes

1. G_{UM} is the maximum unilateral power gain, assuming S_{12} is zero and

$$G_{UM} = 10 \log \frac{|S_{21}|^2}{(1-|S_{11}|^2)(1-|S_{22}|^2)} \text{ dB.}$$

2. I_C = 40 mA; V_{CE} = 8 V; R_L = 50 Ω;
   T_{amb} = 25 °C; f = 900 MHz;
   f_p = 900 MHz; f_q = 902 MHz;
   measured at $f_{(2p-q)}$ = 898 MHz and $f_{(2q-p)}$ = 904 MHz.
3. d_{im} = –60 dB (DIN 45004B);
   $V_p = V_O$; $V_q = V_O$ –6 dB; f_p = 795.25 MHz;
   $V_R = V_O$ –6 dB; f_q = 803.25 MHz; f_r = 805.25 MHz;
   measured at $f_{(p+q-r)}$ = 793.25 MHz; preliminary data.

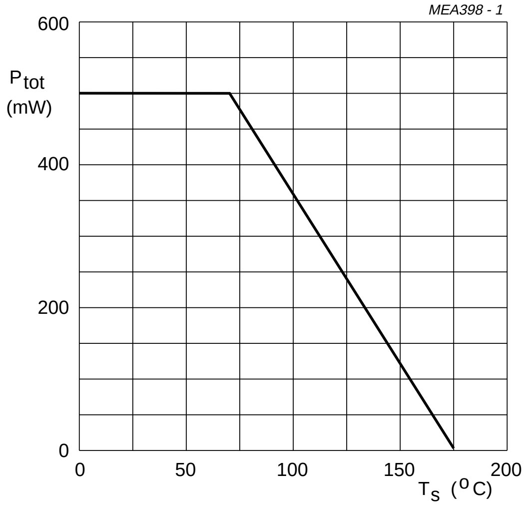
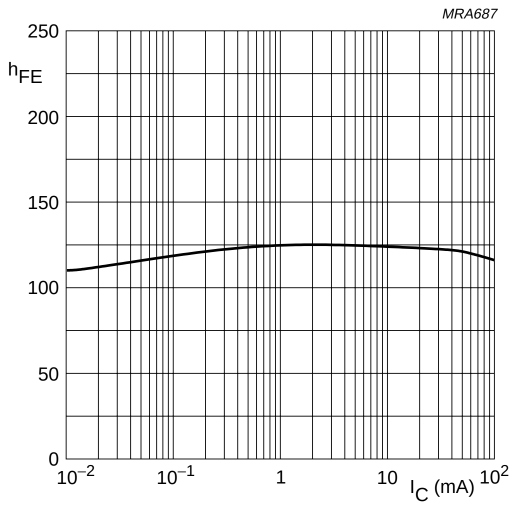
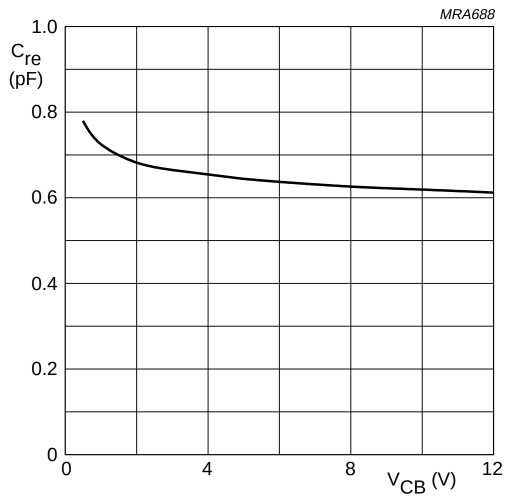


Fig.2 Power derating curve.



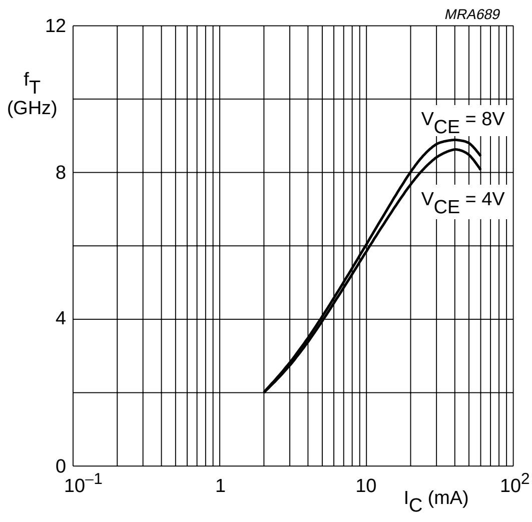
V_{CE} = 8 V.

Fig.3 DC current gain as a function of collector current.



I_C = 0; f = 1 MHz.

Fig.4 Feedback capacitance as a function of collector-base voltage.

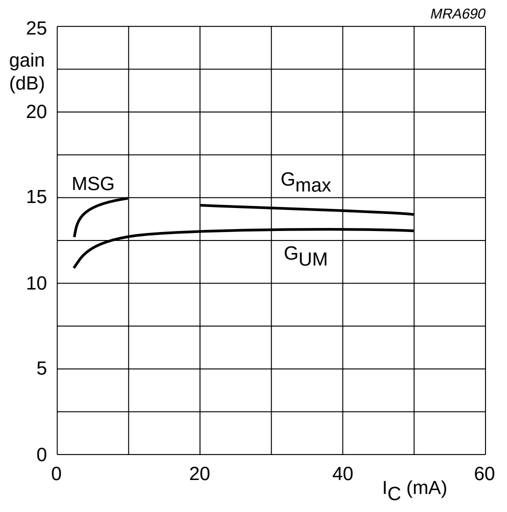


T_{amb} = 25 °C; f = 1 GHz.

Fig.5 Transition frequency as a function of collector current.

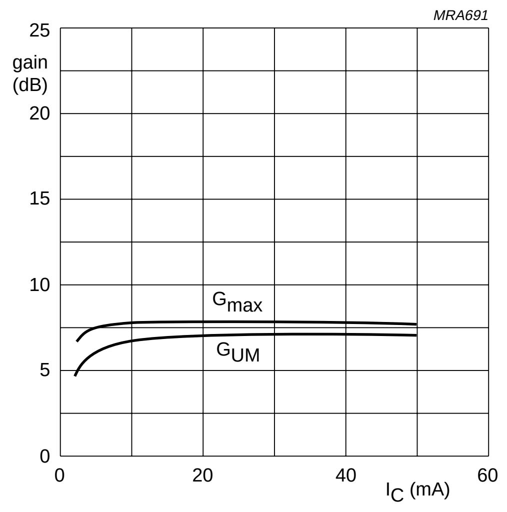
NPN 9 GHz wideband transistor BFR540

In Figs 6 to 9, G_{UM} = maximum unilateral power gain; MSG = maximum stable gain; G_{max} = maximum available gain.



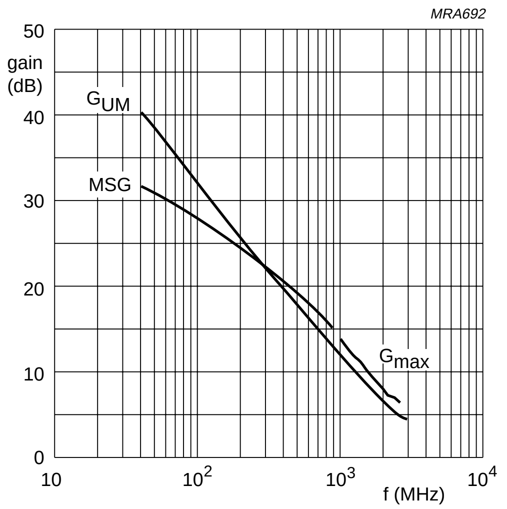
V_{CE} = 8 V; f = 900 MHz.

Fig.6 Gain as a function of collector current.



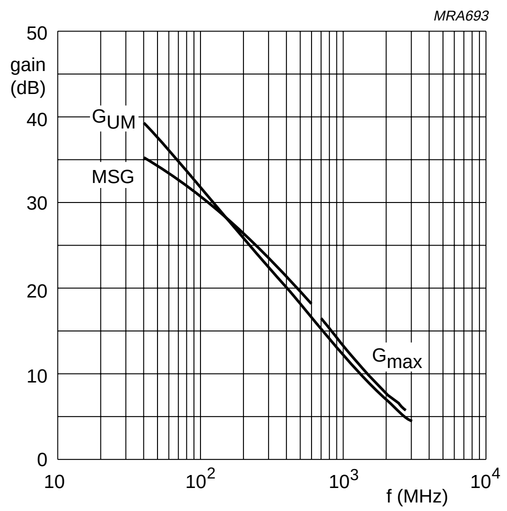
V_{CE} = 8 V; f = 2 GHz.

Fig.7 Gain as a function of collector current.



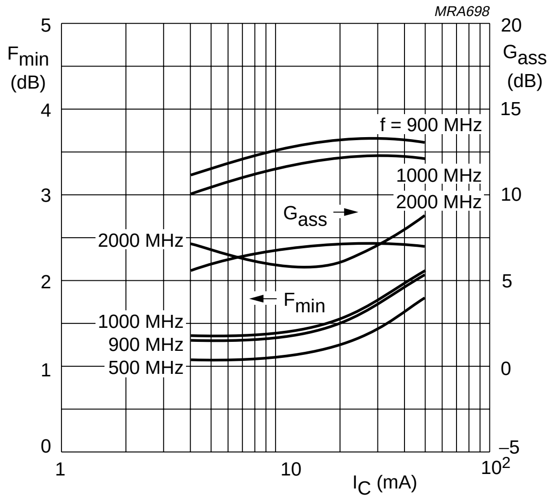
V_{CE} = 8 V; I_c = 10 mA.

Fig.8 Gain as a function of frequency.



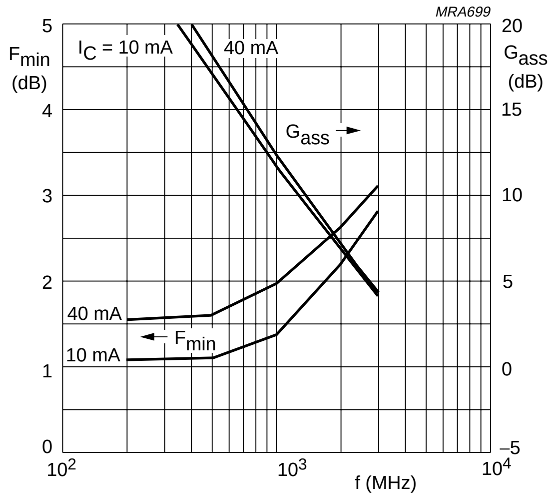
V_{CE} = 8 V; I_c = 40 mA.

Fig.9 Gain as a function of frequency.



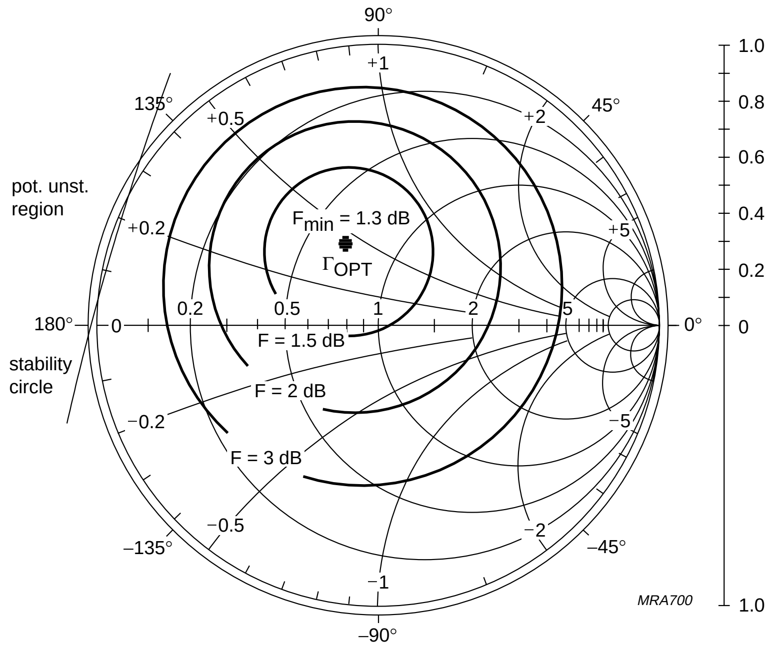
V_{CE} = 8 V.

Fig.10 Minimum noise figure and associated available gain as functions of collector current.



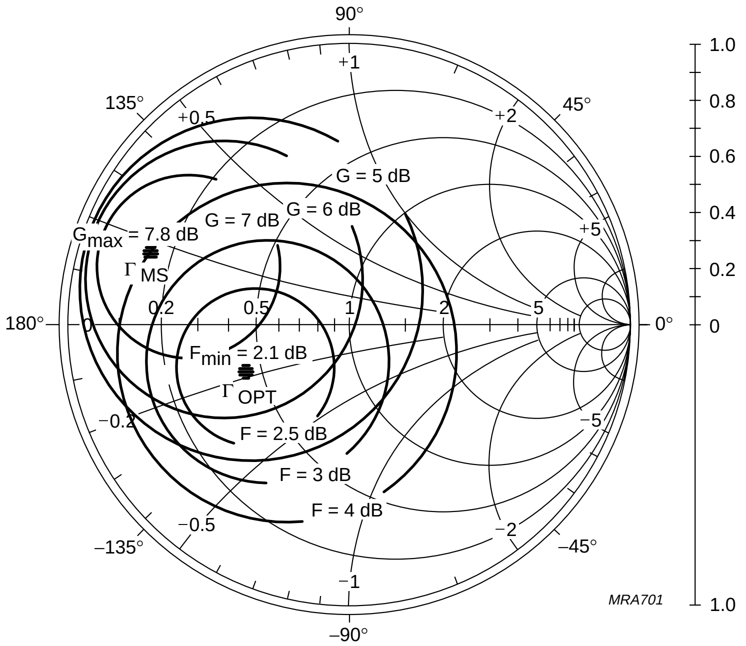
V_{CE} = 8 V.

Fig.11 Minimum noise figure and associated available gain as functions of frequency.



Z_o = 50 Ω.
V_{CE} = 8 V; I_C = 10 mA; f = 900 MHz.

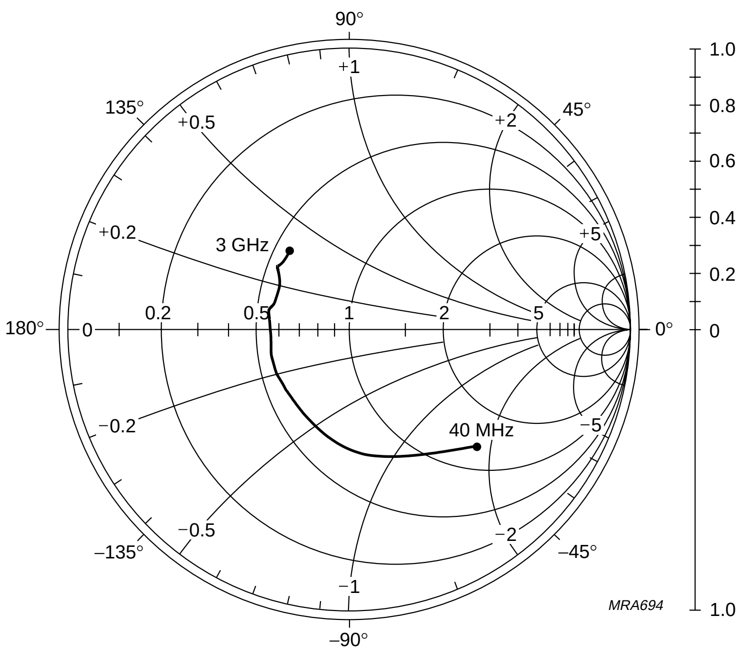
Fig.12 Noise circle figure.



Z_o = 50 Ω.

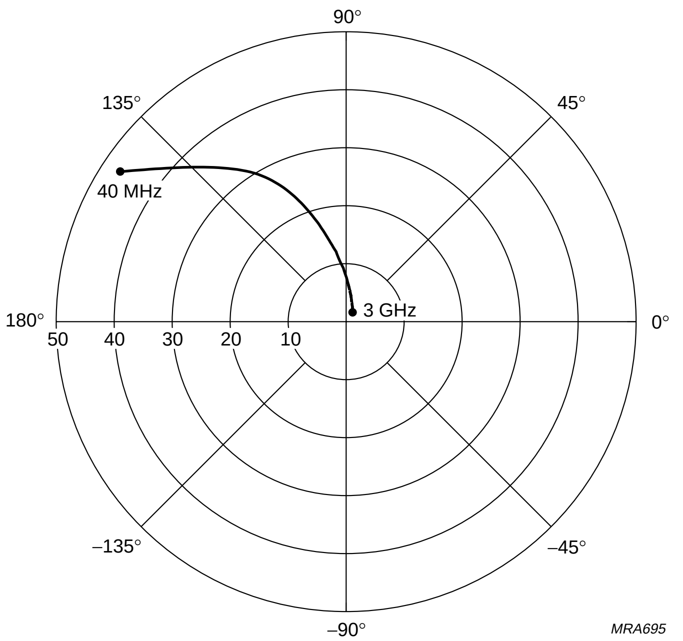
V_{CE} = 8 V; I_C = 10 mA; f = 2000 MHz.

Fig.13 Noise circle figure.



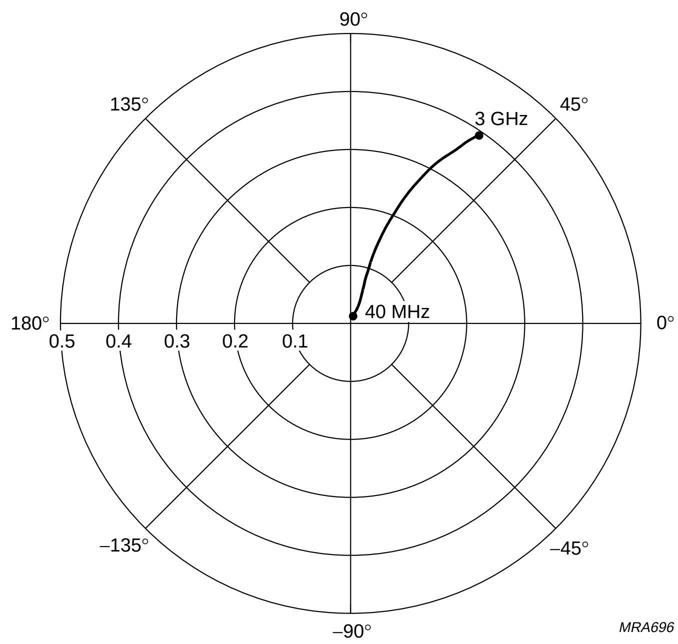
V_{CE} = 8 V; I_C = 40 mA.
Z_o = 50 Ω.

Fig.14 Common emitter input reflection coefficient (S_{11}).



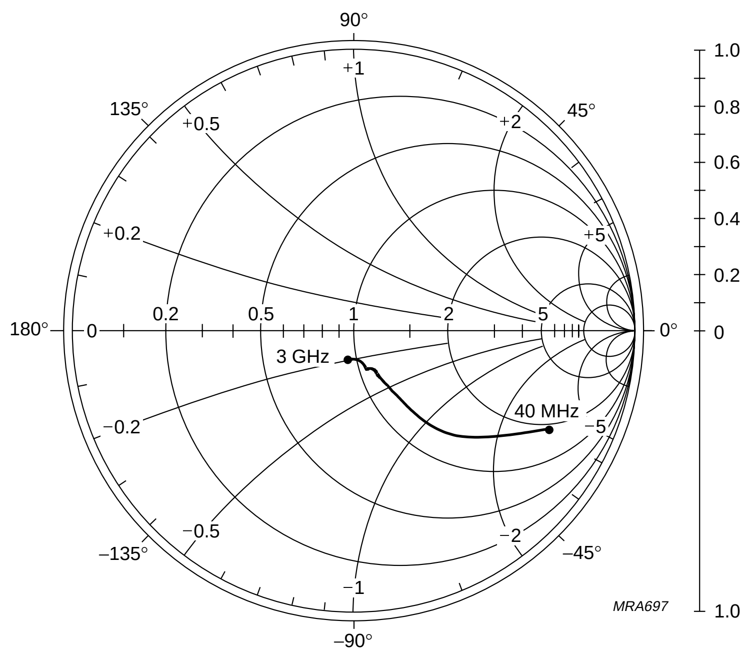
V_{CE} = 8 V; I_C = 40 mA.

Fig.15 Common emitter forward transmission coefficient (S_{21}).



V_{CE} = 8 V; I_C = 40 mA.

Fig.16 Common emitter reverse transmission coefficient (S_{12}).

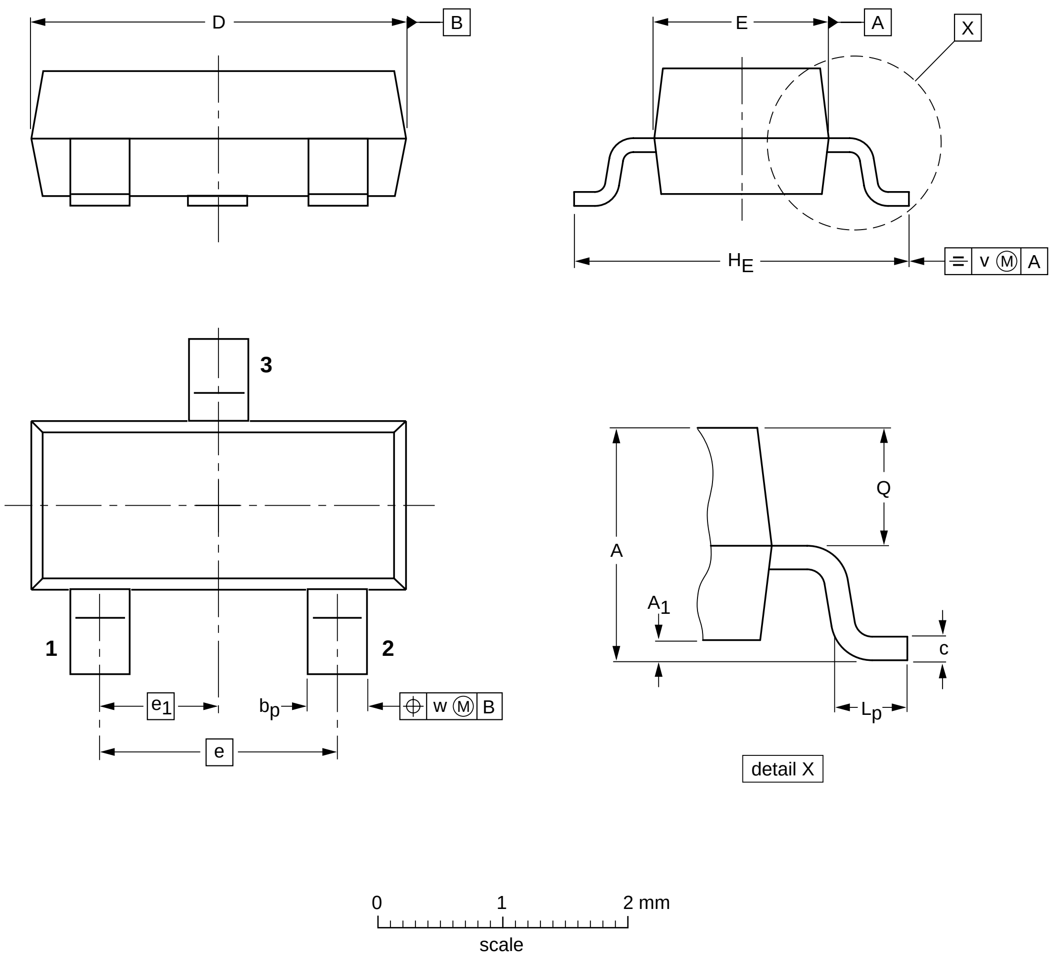


V_{CE} = 8 V; I_C = 40 mA.
Z_o = 50 Ω.

Fig.17 Common emitter output reflection coefficient (S_{22}).

PACKAGE OUTLINE

Plastic surface mounted package; 3 leads **SOT23**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max.	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT23						97-02-28

DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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