DATA SHEET

BLV58
UHF linear push-pull power transistor

Product specification

September 1991

Philips Semiconductors

PHILIPS

UHF linear push-pull power transistor BLV58

FEATURES

- High power gain
- Double stage internal input matching for high input impedance
- Diffused emitter-ballasting resistors enhances ruggedness
- Gold metallization for high reliability.

DESCRIPTION

The BLV58 is a common emitter epitaxial npn silicon planar transistor designed for high linearity class-A operation in UHF (bands 4 and 5) TV transmitters and transposers.

The device is incorporated in a push-pull SOT289 flange envelope with a ceramic cap, which is utilized with the emitters connected to the flange.

PINNING - SOT289

PIN	DESCRIPTION
1	collector 1
2	collector 2
3	base 1
4	base 2
5	emitter

QUICK REFERENCE DATA

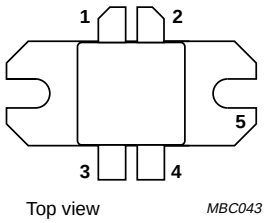
RF performance at T_h = 25 °C in a common emitter test circuit.

MODE OF OPERATION	f_{vision} (MHz)	V_{CE} (V)	I_{CQ} (A)	$P_{o\ sync}$ (W)	G_p (dB)	d_{im} (dB) (note 1)
c.w. class-A	860	25	2×1.6	25	>10	< –45

Note

1. Three-tone test method (vision carrier –8 dB, sound carrier –7 dB, sideband signal –16 dB); zero dB corresponds to peak sync level.

PIN CONFIGURATION



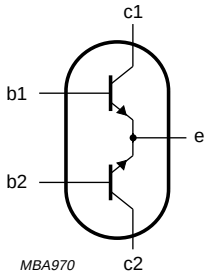


Fig.1 Simplified outline and symbol.

WARNING

Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

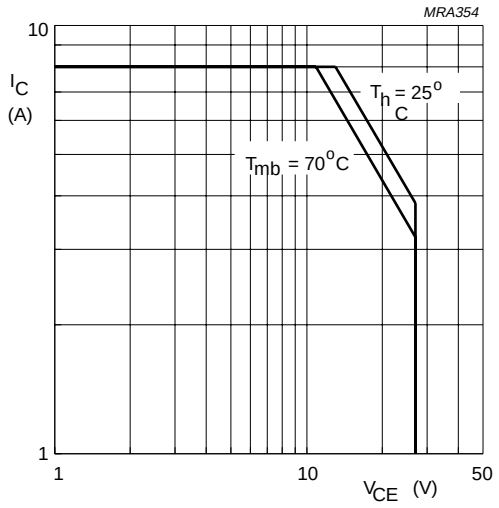
LIMITING VALUES (per transistor section unless otherwise specified)

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	50	V
V_{CEO}	collector-emitter voltage	open base	–	27	V
V_{EBO}	emitter-base voltage	open collector	–	3.5	V
I_C, $I_{C(AV)}$	collector current	DC or average value	–	4	A
I_{CM}	collector current	peak value; f > 1 MHz	–	8	A
P_{tot}	total power dissipation	DC operation; T_{mb} = 70 °C (note 1)	–	87	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction operating temperature		–	200	°C

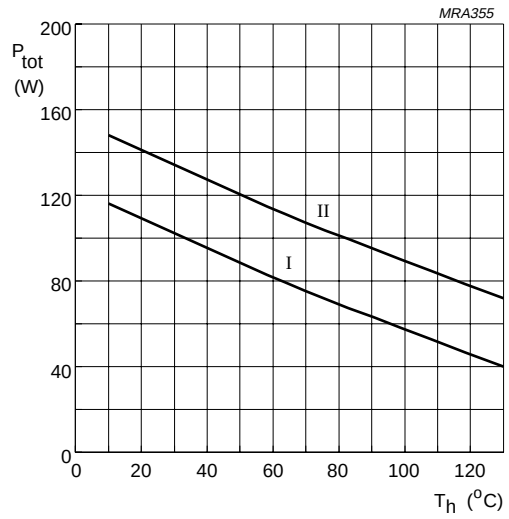
Note

1. Total device, both sections equally loaded.



Total device, both sections equally loaded.

Fig.2 DC SOAR.



(I) Continuous DC operation.
(II) Short time operation during mismatch.
Total device, both sections equally loaded.

Fig.3 Power derating curve.

THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$R_{th\ j\text{-}mb(DC)}$	from junction to mounting base	P_{dis} = 87 W; T_{mb} = 70 °C (note 1)	1.5	K/W
$R_{th\ mb\text{-}h}$	from mounting base to heatsink	note 1	0.2	K/W

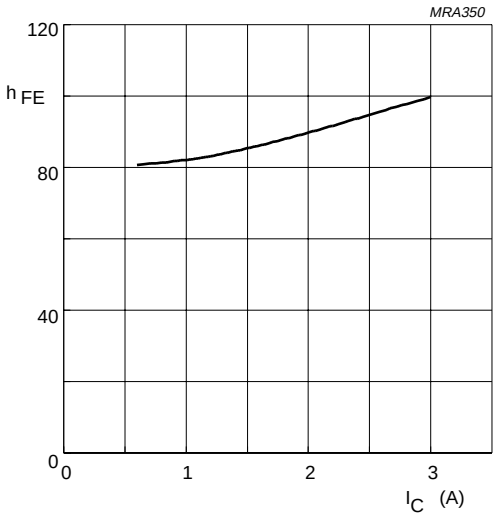
Note

1. Total device, both sections equally loaded.

CHARACTERISTICS

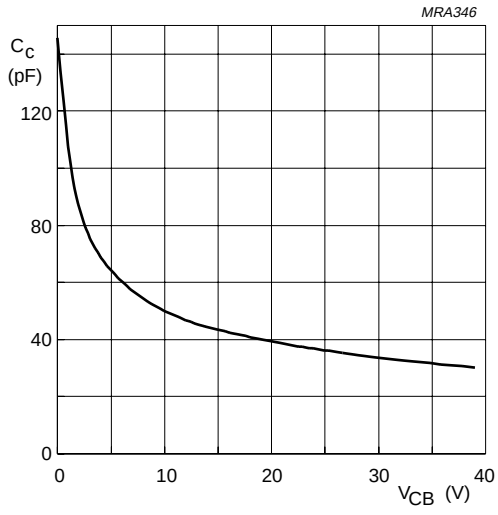
Values apply to either transistor section; T_j = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	open emitter; I_C = 20 mA	50	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	open base; I_C = 50 mA	27	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	open collector; I_E = 10 mA	3.5	–	–	V
I_{CES}	collector-emitter leakage current	V_{BE} = 0; V_{CE} = 27 V	–	–	10	mA
h_{FE}	DC current gain	V_{CE} = 25 V; I_C = 1.6 A	30	–	–	
C_c	collector capacitance	V_{CB} = 25 V; $I_E = I_e$ = 0; f = 1 MHz	–	36	45	pF



V_{CE} = 25 V.

Fig.4 DC current gain as a function of collector current, typical values.



$I_E = i_e = 0$; f = 1 MHz.

Fig.5 Collector capacitance as a function of collector-base voltage, typical values.

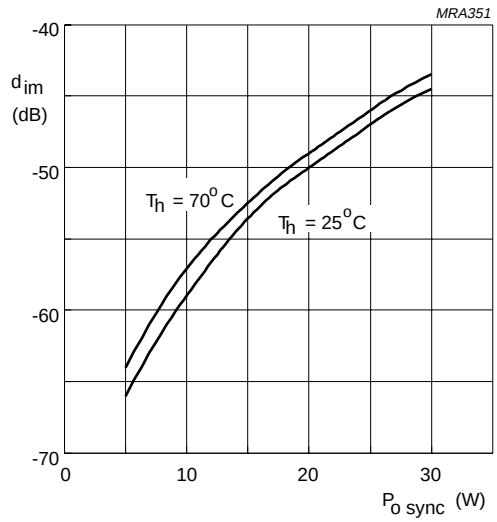
APPLICATION INFORMATION

RF performance at T_h = 25 °C in a common emitter push-pull test circuit; $R_{th\ mb\text{-}h}$ = 0.2 K/W.

MODE OF OPERATION	f_{vision} (MHz)	V_{CE} (V)	I_{CQ} (A)	$P_{o\ sync}$ (W)	G_P (dB)	d_{im} (dB) (note 1)	d_{cm} (%) (note 2)
c.w. class-A	860	25	2 × 1.6	25	> 10 typ. 11.5	< –45 typ. –47	< 20

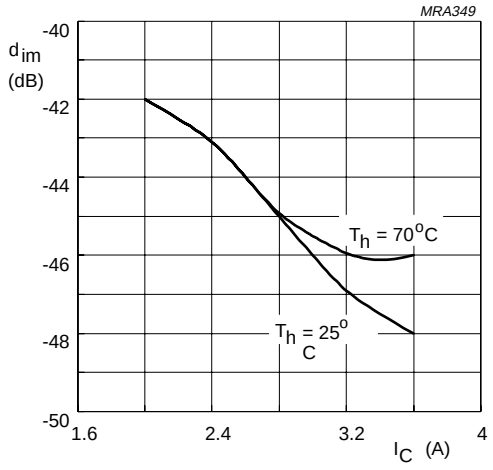
Notes

1. Three-tone test method: vision carrier –8 dB (860 MHz), sound carrier –7 dB (865.5 MHz), sideband signal –16 dB (861 MHz); zero dB corresponds to peak sync level.
2. Two-tone test method: vision carrier 0 dB (860 MHz), sound carrier –7 dB (865.5 MHz); zero dB corresponds to peak sync level. Cross-modulation distortion (d_{cm}) is the voltage variation (%) of the sound carrier when the vision carrier is switched from 0 dB to –20 dB.



Class-A operation; V_{CE} = 25 V; f = 860 MHz; 3-tone test (–8 dB, –16 dB, –7 dB); I_{CQ} = 2 × 1.6 A.

Fig.6 Intermodulation distortion as a function of output power.



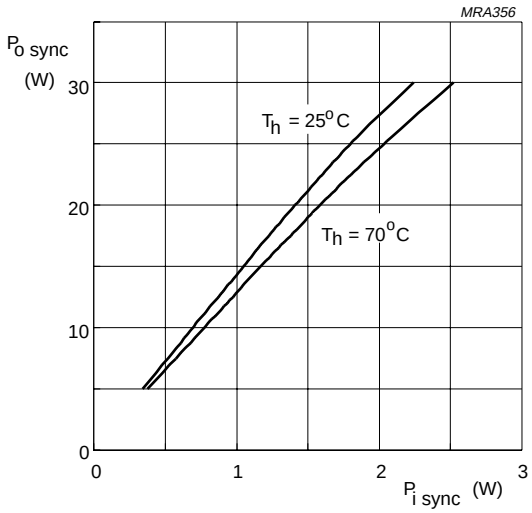
Class-A operation; V_{CE} = 25 V; f = 860 MHz; 3-tone test (–8 dB, –16 dB, –7 dB); $P_{o\ sync}$ = 25 W.

Fig.7 Intermodulation distortion as a function of collector current.

Ruggedness in Class-A operation

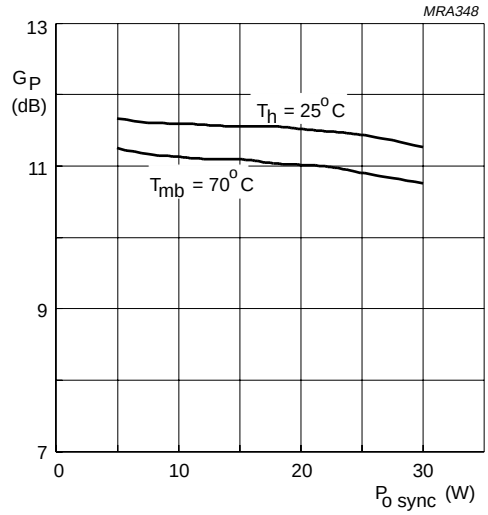
The BLV58 is capable of withstanding a full load mismatch corresponding to VSWR = 50:1 through all phases under the following conditions:

V_{CE} = 25 V, f = 860 MHz, T_h = 25 °C, $R_{th\ mb\text{-}h}$ = 0.2 K/W, I_{CQ} = 2 × 1.6 A, and rated output power.



Class-A operation; V_{CE} = 25 V; f = 860 MHz; 3-tone test (–8 dB, –16 dB, –7 dB); $I_{CQ} = 2 \times 1.6$ A.

Fig.8 Output power as a function of input power.



Class-A operation; V_{CE} = 25 V; f = 860 MHz; 3-tone test (–8 dB, –16 dB, –7 dB); $I_{CQ} = 2 \times 1.6$ A.

Fig.9 Gain as a function of output power, typical values.

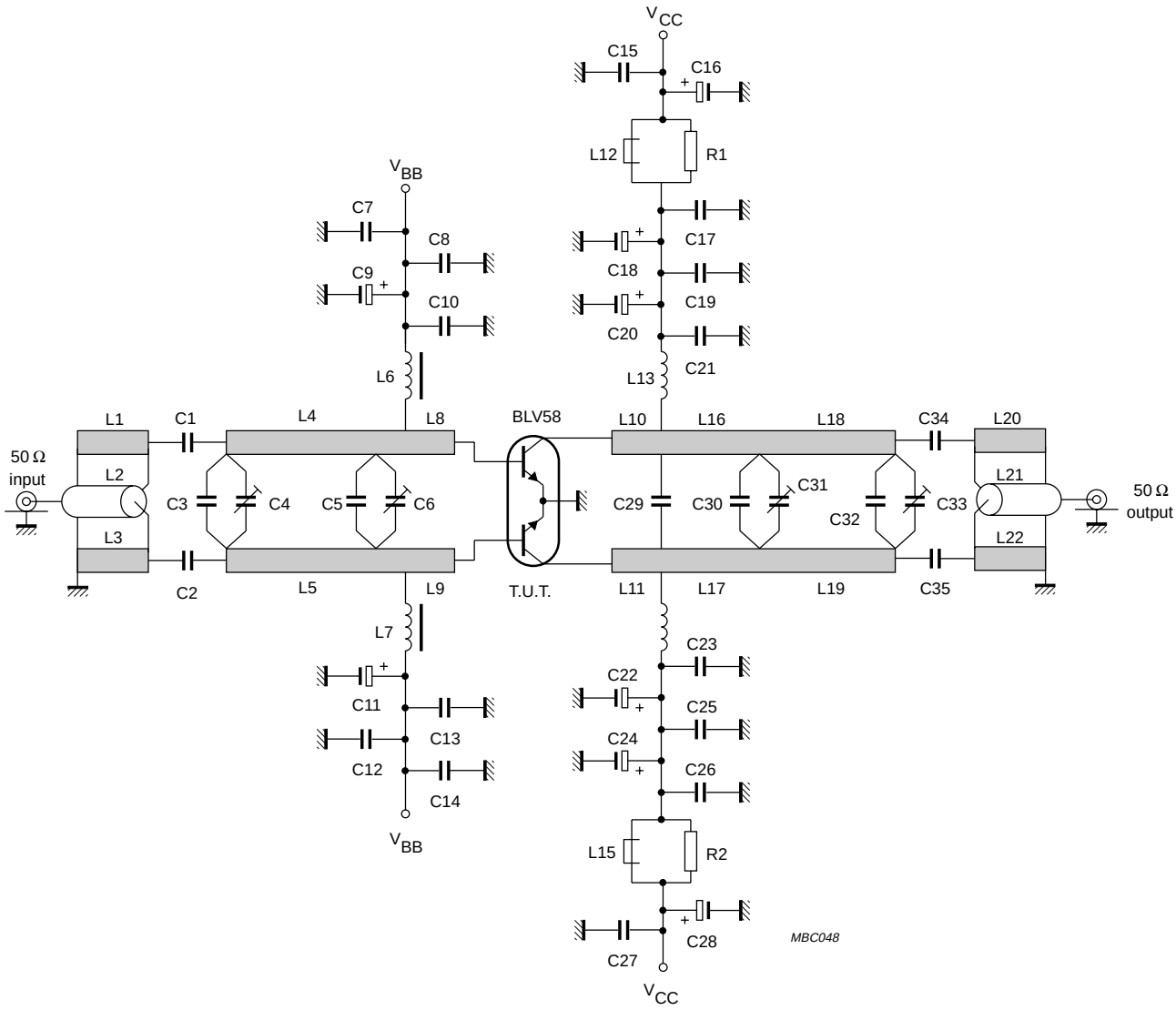


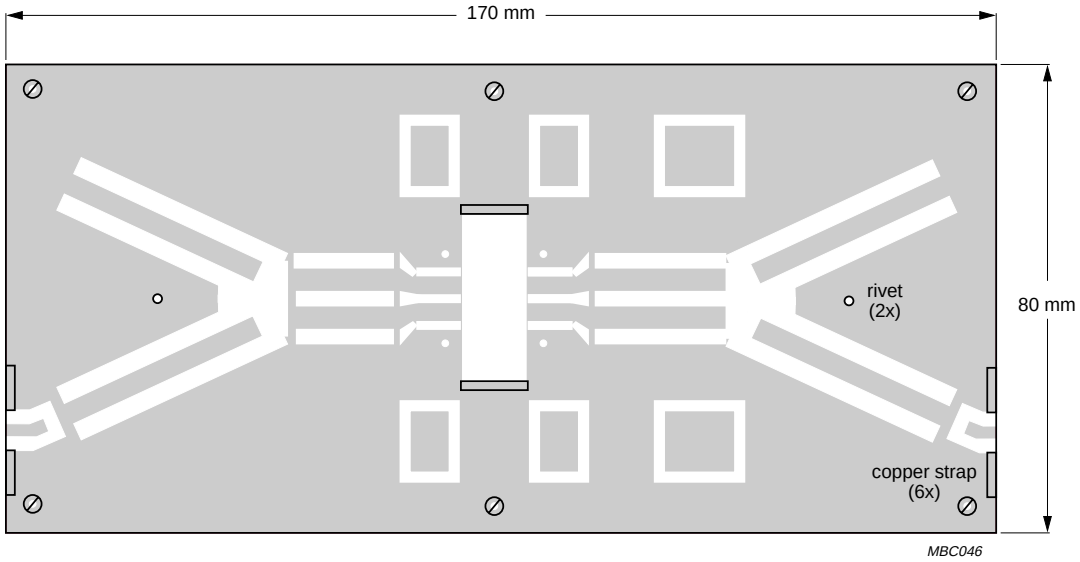
Fig.10 Class-A test circuit at f = 860 MHz.

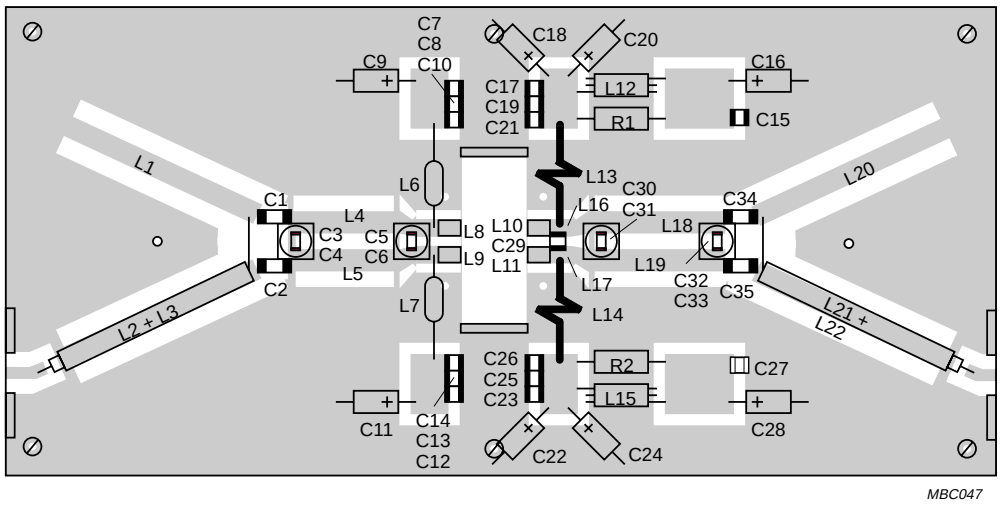
List of components (see test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2, C34, C35	multilayer ceramic chip capacitor (note 1)	15 pF		
C3	multilayer ceramic chip capacitor (note 1)	3.9 pF		
C4, C6	film dielectric trimmer	5.5 pF		2222 809 09005
C5	multilayer ceramic chip capacitor (note 1)	7.5 pF		
C7, C12, C17, C26	multilayer ceramic chip capacitor	10 nF		2222 852 47103
C8, C14, C19, C25	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C9, C11, C16, C20, C22, C28	63 V electrolytic capacitor	10 μF		
C10, C13, C15, C21, C23, C27	multilayer ceramic chip capacitor (note 1)	330 pF		
C18, C24	63 V electrolytic capacitor	1 μF		
C29	multilayer ceramic chip capacitor (note 1)	12 pF		
C30	multilayer ceramic chip capacitor (note 1)	5.6 pF		
C31, C33	film dielectric trimmer	3.5 pF		2222 809 05001
C32	multilayer ceramic chip capacitor (note 1)	2.7 pF		
L1, L3, L20, L22	stripline (note 2)	35 Ω	39 mm × 4 mm	
L2, L21	semi-rigid cable (note 3)	50 Ω	ext. dia. 3.6 mm; length 39 mm	
L4, L5	stripline (note 2)	38 Ω	19 mm × 3.5 mm	
L6, L7	RF choke	470 nH		
L8, L9	stripline (note 2)	38 Ω	7.5 mm × 3.5 mm	
L10, L11	stripline (note 2)	38 Ω	4.5 mm × 3.5 mm	
L12, L15	grade 3B RF choke			4312 020 36642
L13, L14	1 turn 1.5 mm copper wire	14 nH	int. dia 7 mm; leads 2 × 6 mm	
L16, L17	stripline (note 2)	38 Ω	7 mm × 3.5 mm	
L18, L19	stripline (note 2)	38 Ω	18 mm × 3.5 mm	
R1, R2	1 W metal film resistor	10 Ω		

Notes

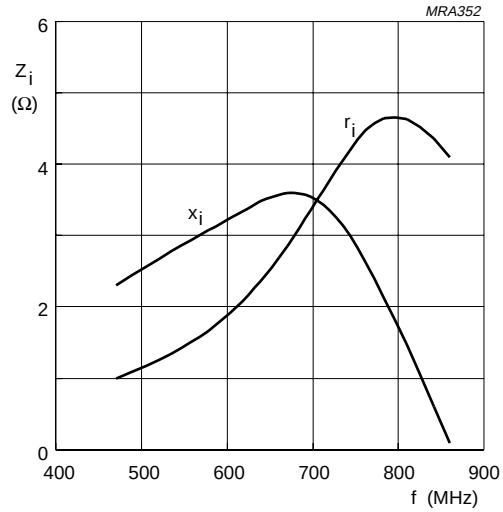
1. American Technical Ceramics type 100B or capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with PTFE microfibre-glass dielectric (ε_r = 2.2), thickness $^1/_{32}$ inch, thickness of copper sheet 2 × 35 μm.
3. Cables L2 and L21 are soldered to striplines L1 and L20, respectively.





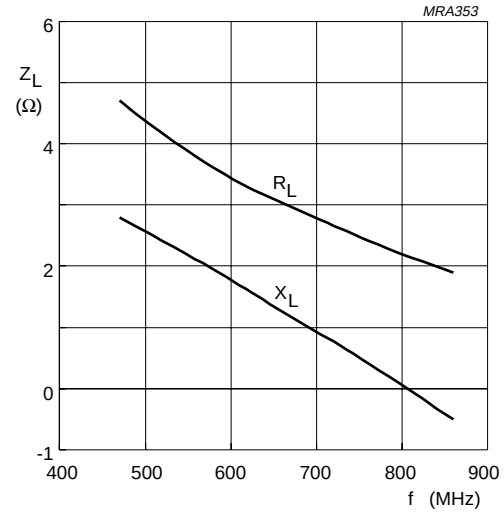
The components are mounted on one side of a copper clad PTFE microfibre-glass board; the other side is unetched and serves as a ground plane. Earth connections from the component side to the ground plane are made by hollow rivets and copper straps.

Fig.11 Component layout for 860 MHz class-A test circuit.



Class-A operation; V_{CE} = 25 V;
I_{CQ} = 1.6 A (per section); P_L = 25 W (total device);
T_h = 25 °C.

Fig.12 Input impedance per section (series components) as a function of frequency, typical values.



Class-A operation; V_{CE} = 25 V;
I_{CQ} = 1.6 A (per section); P_L = 25 W (total device);
T_h = 25 °C.

Fig.13 Load impedance per section (series components) as a function of frequency, typical values.

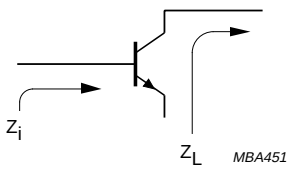
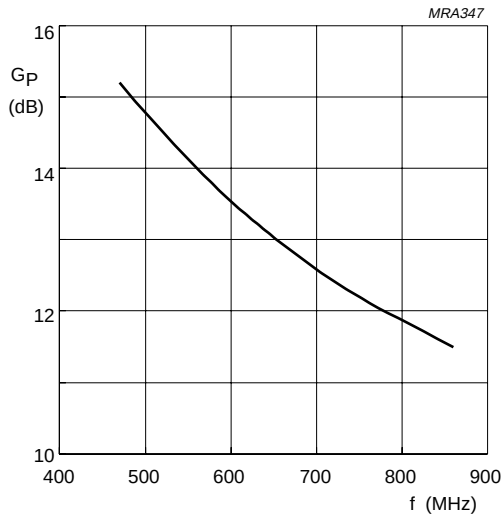


Fig.14 Definition of transistor impedance.

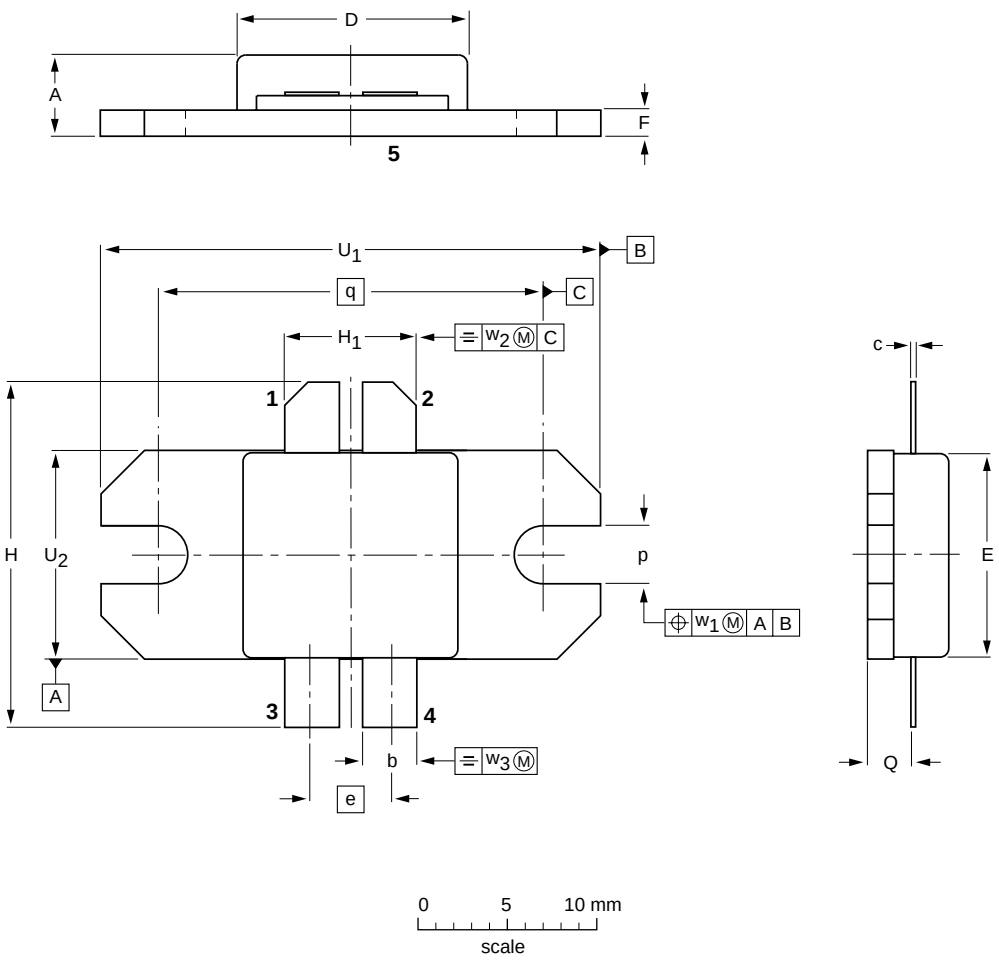


Class-A operation; V_{CE} = 25 V;
I_{CQ} = 1.6 A (per section); P_L = 25 W (total device);
T_h = 25 °C.

Fig.15 Power gain as a function of frequency, typical values.

PACKAGE OUTLINE

Flanged ceramic package; 2 mounting holes; 4 leads **SOT289A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	E	e	F	H	H_1	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	4.65 3.92	3.33 3.07	0.10 0.05	13.10 12.90	11.53 11.33	4.60	1.65 1.40	19.81 19.05	4.85 4.34	3.43 3.17	2.31 2.06	21.44	28.07 27.81	11.81 11.56	0.51	1.02	0.25
inches	0.183 0.154	0.131 0.121	0.004 0.002	0.516 0.508	0.454 0.446	0.181	0.065 0.055	0.780 0.750	0.191 0.171	0.135 0.125	0.091 0.081	0.844	1.105 1.095	0.465 0.455	0.02	0.04	0.01

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT289A						97-06-28

DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.