



# Very Low Power/Voltage CMOS SRAM 512K X 16 bit

## BS616LV8015

### ■ FEATURES

- Very low operation voltage : 4.5~5.5V
- Very low power consumption :
  - Vcc = 5.0V C-grade: 45mA (Max.) operating current
  - I-grade : 50mA (Max.) operating current
  - 3uA (Typ.) CMOS standby current
- High speed access time :
  - 55 70ns (Max.) at Vcc=5V
  - 70 70ns (Max.) at Vcc=5V
- Automatic power down when chip is deselected
- Three state outputs and TTL compatible
- Fully static operation
- Data retention supply voltage as low as 1.5V
- Easy expansion with CE1, CE2 and OE options
- I/O Configuration x8/x16 selectable by LB and UB pin

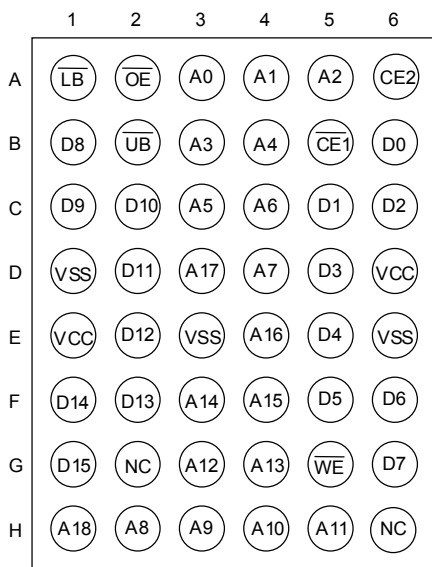
### ■ DESCRIPTION

The BS616LV8015 is a high performance, very low power CMOS Static Random Access Memory organized as 524,288 words by 16 bits and operates from a wide range of 4.5V to 5.5V supply voltage. Advanced CMOS technology and circuit techniques provide both high speed and low power features with a typical CMOS standby current of 3uA and maximum access time of 55/70ns in 5V operation. Easy memory expansion is provided by an active LOW chip enable( $\overline{CE1}$ ), active HIGH chip enable (CE2), active LOW output enable( $\overline{OE}$ ) and three-state output drivers. The BS616LV8015 has an automatic power down feature, reducing the power consumption significantly when chip is deselected. The BS616LV8015 is available in 48-pin BGA package.

### ■ PRODUCT FAMILY

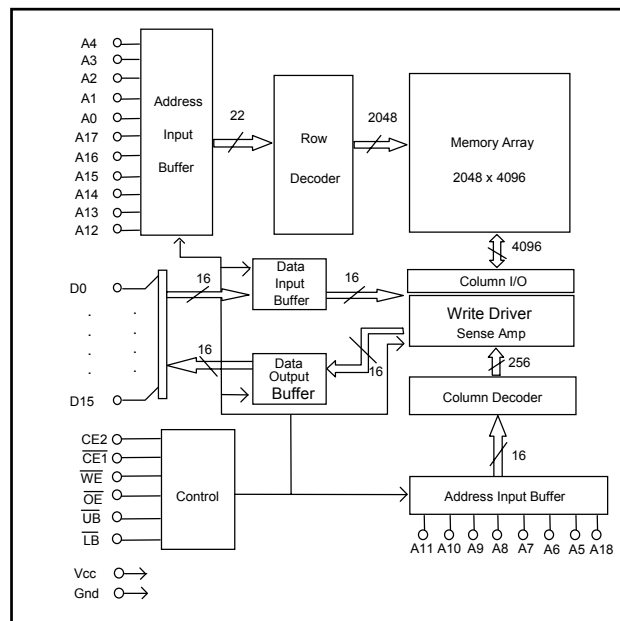
PRODUCT FAMILY	OPERATING TEMPERATURE	Vcc RANGE	SPEED (ns)	POWER DISSIPATION		PKG TYPE
				STANDBY (IccsB1, Max)	Operating (Icc, Max)	
				Vcc=5V	Vcc=5V	
BS616LV8015BC	+0°C to +70°C	4.5V ~ 5.5V	55 / 70	30uA	45mA	BGA-48-0810
BS616LV8015BI	-40°C to +85°C	4.5V ~ 5.5V	55 / 70	100uA	50mA	BGA-48-0810

### ■ PIN CONFIGURATIONS



48-Ball CSP top View

### ■ BLOCK DIAGRAM



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**■ PIN DESCRIPTIONS**

Name	Function
<b>A0-A18 Address Input</b>	These 19 address inputs select one of the 524,288 x 16-bit words in the RAM.
<b><math>\overline{CE1}</math> Chip Enable 1 Input <math>CE2</math> Chip Enable 2 Input</b>	$\overline{CE1}$ is active LOW and $CE2$ is active HIGH. Both chip enables must be active when data read from or write to the device. If either chip enable is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high impedance state when the device is deselected.
<b><math>\overline{WE}</math> Write Enable Input</b>	The write enable input is active LOW and controls read and write operations. With the chip selected, when $\overline{WE}$ is HIGH and $\overline{OE}$ is LOW, output data will be present on the DQ pins; when $\overline{WE}$ is LOW, the data present on the DQ pins will be written into the selected memory location.
<b><math>\overline{OE}</math> Output Enable Input</b>	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{OE}$ is inactive.
<b><math>\overline{LB}</math> and <math>\overline{UB}</math> Data Byte Control Input</b>	Lower byte and upper byte data input/output control pins.
<b>D0 - D15 Data Input/Output Ports</b>	These 16 bi-directional ports are used to read data from or write data into the RAM.
<b>Vcc</b>	Power Supply
<b>Gnd</b>	Ground

**■ TRUTH TABLE**

MODE	$\overline{CE1}$	$CE2$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	D0~D7	D8~D15	Vcc CURRENT
Not selected (Power Down)	H	X	X	X	X	X	High Z	High Z	$I_{CCSB}, I_{CCSB1}$
	X	L	X	X	X	X	High Z	High Z	$I_{CCSB}, I_{CCSB1}$
Output Disabled	L	H	H	H	X	X	High Z	High Z	$I_{CC}$
Read	L	H	H	L	L	L	Dout	Dout	$I_{CC}$
					H	L	High Z	Dout	$I_{CC}$
					L	H	Dout	High Z	$I_{CC}$
Write	L	H	L	X	L	L	Din	Din	$I_{CC}$
					H	L	X	Din	$I_{CC}$
					L	H	Din	X	$I_{CC}$

**■ ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

SYMBOL	PARAMETER	RATING	UNITS
V TERM	Terminal Voltage with Respect to GND	-0.5 to Vcc+0.5	V
T BIAS	Temperature Under Bias	-40 to +125	°C
T STG	Storage Temperature	-60 to +150	°C
P T	Power Dissipation	1.0	W
I OUT	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**■ OPERATING RANGE**

RANGE	AMBIENT TEMPERATURE	Vcc
Commercial	0 °C to +70 °C	4.5V ~ 5.5V
Industrial	-40 °C to +85 °C	4.5V ~ 5.5V

**■ CAPACITANCE <sup>(1)</sup> (TA = 25°C, f = 1.0 MHz)**

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
CIN	Input Capacitance	VIN=0V	6	pF
CDQ	Input/Output Capacitance	VI/O=0V	8	pF

1. This parameter is guaranteed and not tested.

**DC ELECTRICAL CHARACTERISTICS ( TA = 0 to + 70°C )**

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MIN. TYP. <sup>(1)</sup> MAX.			UNITS
V <sub>IL</sub>	Guaranteed Input Low Voltage (2)	V <sub>CC</sub> =5V	-0.5	--	0.8	V
V <sub>IH</sub>	Guaranteed Input High Voltage (2)	V <sub>CC</sub> =5V	2.2	--	V <sub>CC</sub> +0.2	V
I <sub>IL</sub>	Input Leakage Current	V <sub>CC</sub> = Max, V <sub>IN</sub> = 0V to V <sub>CC</sub>	--	--	1	uA
I <sub>OL</sub>	Output Leakage Current	V <sub>CC</sub> = Max, $\overline{CE1}=V_{IH}$ , or CE2 = V <sub>IL</sub> , or OE = V <sub>IH</sub> , V <sub>I/O</sub> = 0V to V <sub>CC</sub>	--	--	1	uA
V <sub>OL</sub>	Output Low Voltage	V <sub>CC</sub> = Max, I <sub>OL</sub> = 2mA	--	--	0.4	V
V <sub>OH</sub>	Output High Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = -1mA	2.4	--	--	V
I <sub>CC</sub>	Operating Power Supply Current	V <sub>CC</sub> = max, $\overline{CE1}=V_{IL}$ and CE2 = V <sub>IH</sub> , I <sub>DQ</sub> = 0mA, F = F <sub>max</sub> (3)	--	--	45	mA
I <sub>CCSB</sub>	Standby Current - TTL	V <sub>CC</sub> = max, $\overline{CE1} = V_{IH}$ or CE2 = V <sub>IL</sub> , I <sub>DQ</sub> = 0mA	--	--	2	mA
I <sub>CCSB1</sub>	Standby Current - CMOS	V <sub>CC</sub> = max, $\overline{CE1} \geq V_{CC} - 0.2V$ , or CE2 $\leq 0.2V$ , V <sub>IN</sub> $\geq V_{CC} - 0.2V$ or V <sub>IN</sub> $\leq 0.2V$	--	3	30	uA

1. Typical characteristics are at TA = 25°C.

2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.

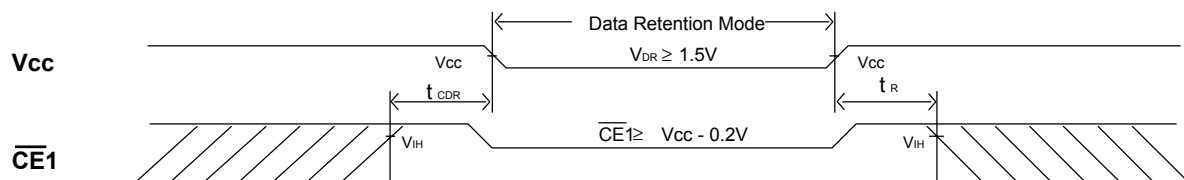
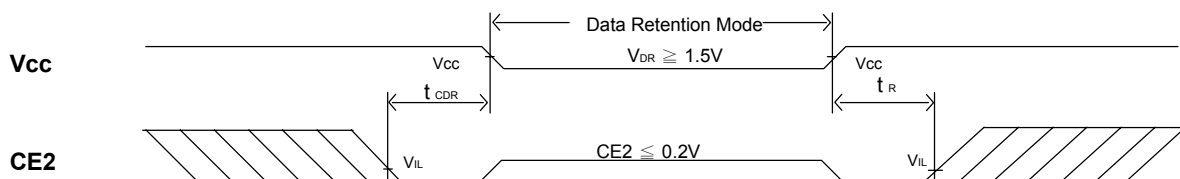
3. F<sub>max</sub> = 1/t<sub>RC</sub>.

**DATA RETENTION CHARACTERISTICS ( TA = 0 to + 70°C )**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN. TYP. (1) MAX.			UNITS
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention	$\overline{CE1} \geq V_{CC} - 0.2V$ or CE2 $\leq 0.2V$ V <sub>IN</sub> $\geq V_{CC} - 0.2V$ or V <sub>IN</sub> $\leq 0.2V$	1.5	--	--	V
I <sub>CCDR</sub>	Data Retention Current	$\overline{CE1} \geq V_{CC} - 0.2V$ or CE2 $\leq 0.2V$ V <sub>IN</sub> $\geq V_{CC} - 0.2V$ or V <sub>IN</sub> $\leq 0.2V$	--	0.2	2	uA
t <sub>CDR</sub>	Chip Deselect to Data Retention Time	See Retention Waveform	0	--	--	ns
t <sub>R</sub>	Operation Recovery Time		T <sub>RC</sub> (2)	--	--	ns

1. V<sub>CC</sub> = 1.5V, T<sub>A</sub> = + 25°C

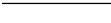
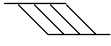



2. t<sub>RC</sub> = Read Cycle Time

**LOW V<sub>CC</sub> DATA RETENTION WAVEFORM (1) (  $\overline{CE1}$  Controlled )**

**LOW V<sub>CC</sub> DATA RETENTION WAVEFORM (2) ( CE2 Controlled )**


## AC TEST CONDITIONS

Input Pulse Levels	Vcc/0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Level	0.5Vcc

## KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	MUST BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGE FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGE FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGE: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

## AC TEST LOADS AND WAVEFORMS

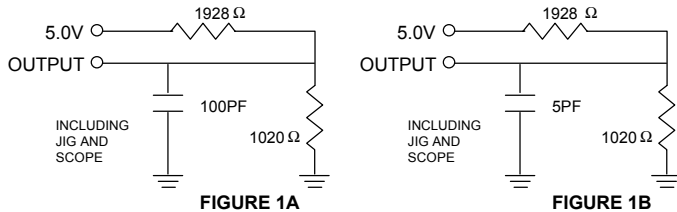


FIGURE 1A

FIGURE 1B

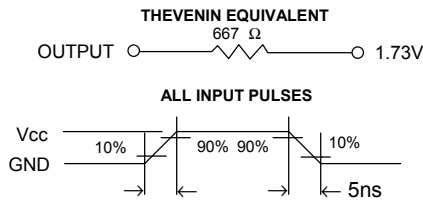


FIGURE 2

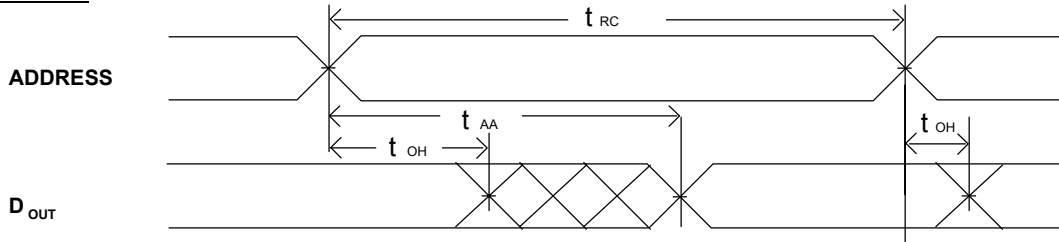
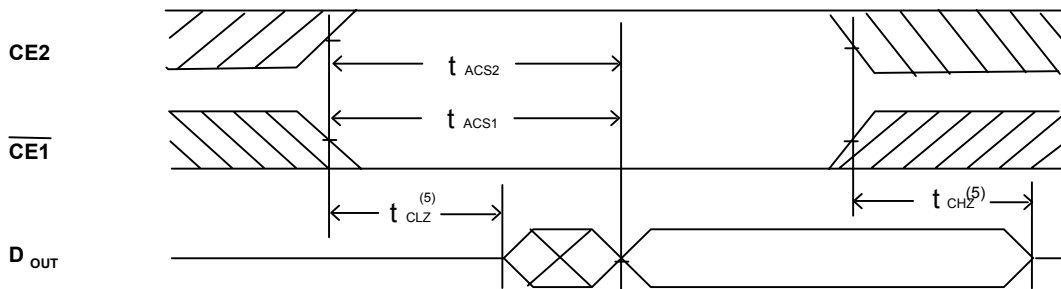
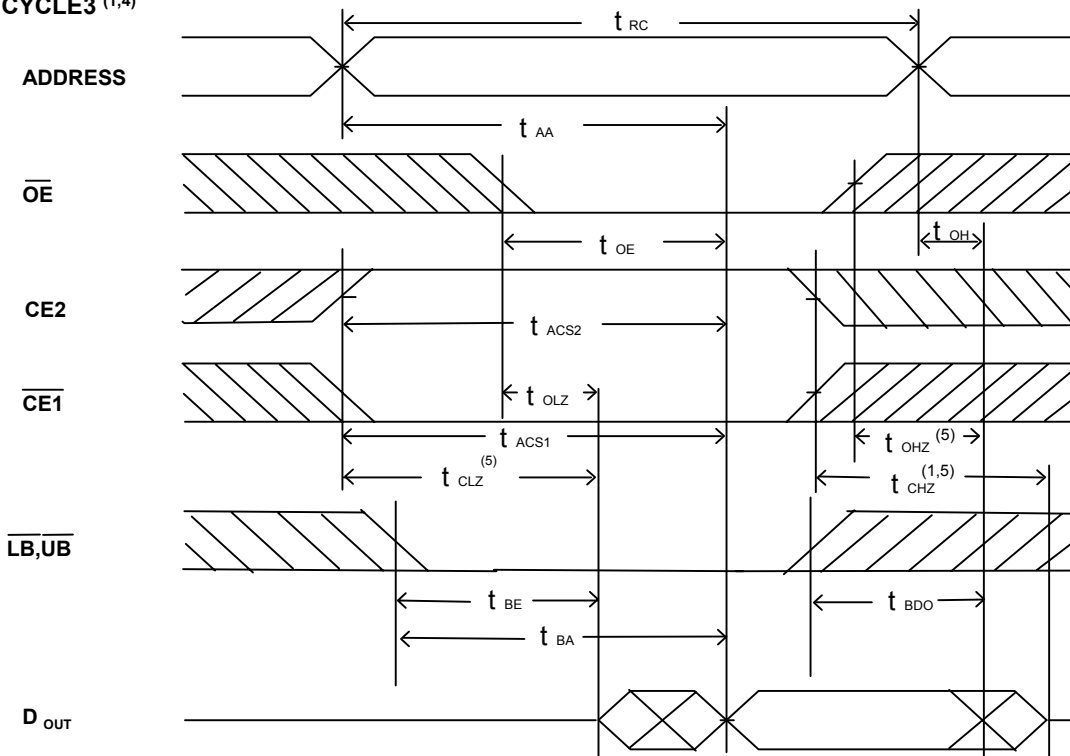
## AC ELECTRICAL CHARACTERISTICS (TA = 0 to + 70°C, Vcc=5V)

### READ CYCLE

JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION	BS616LV8015-70			BS616LV8015-55			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
t <sub>AVAX</sub>	t <sub>RC</sub>	Read Cycle Time	70	--	--	55	--	--	ns
t <sub>AVQV</sub>	t <sub>AA</sub>	Address Access Time	--	--	70	--	--	55	ns
t <sub>ELQV</sub>	t <sub>ACS1</sub>	Chip Select Access Time (CE1)	--	--	70	--	--	55	ns
t <sub>ELQV</sub>	t <sub>ACS2</sub>	Chip Select Access Time (CE2)	--	--	70	--	--	55	ns
t <sub>BA</sub>	t <sub>BA</sub> <sup>(1)</sup>	Data Byte Control Access Time (LB,UB)	--	--	35	--	--	30	ns
t <sub>GLQV</sub>	t <sub>OE</sub>	Output Enable to Output Valid	--	--	35	--	--	30	ns
t <sub>ELQX</sub>	t <sub>CLZ</sub>	Chip Select to Output Low Z (CE2,CE1)	10	--	--	10	--	--	ns
t <sub>BE</sub>	t <sub>BE</sub>	Data Byte Control to Output Low Z (LB,UB)	10	--	--	10	--	--	ns
t <sub>GLQX</sub>	t <sub>OLZ</sub>	Output Enable to Output in Low Z	10	--	--	10	--	--	ns
t <sub>EHQZ</sub>	t <sub>CHZ</sub>	Chip Deselect to Output in High Z (CE2,CE1)	0	--	35	0	--	30	ns
t <sub>BDO</sub>	t <sub>BDO</sub>	Data Byte Control to Output High Z (LB,UB)	0	--	35	0	--	30	ns
t <sub>GHQZ</sub>	t <sub>OHZ</sub>	Output Disable to Output in High Z	0	--	30	0	--	25	ns
t <sub>AXOX</sub>	t <sub>OH</sub>	Output Disable to Address Change	10	--	--	10	--	--	ns

NOTE :

- t<sub>BA</sub> is 35ns/30ns (@speed=70ns/55ns) with address toggle .  
t<sub>BA</sub> is 70ns/55ns (@speed=70ns/55ns) without address toggle .

**SWITCHING WAVEFORMS (READ CYCLE)**
**READ CYCLE1 (1,2,4)**

**READ CYCLE2 (1,3,4)**

**READ CYCLE3 (1,4)**

**NOTES:**

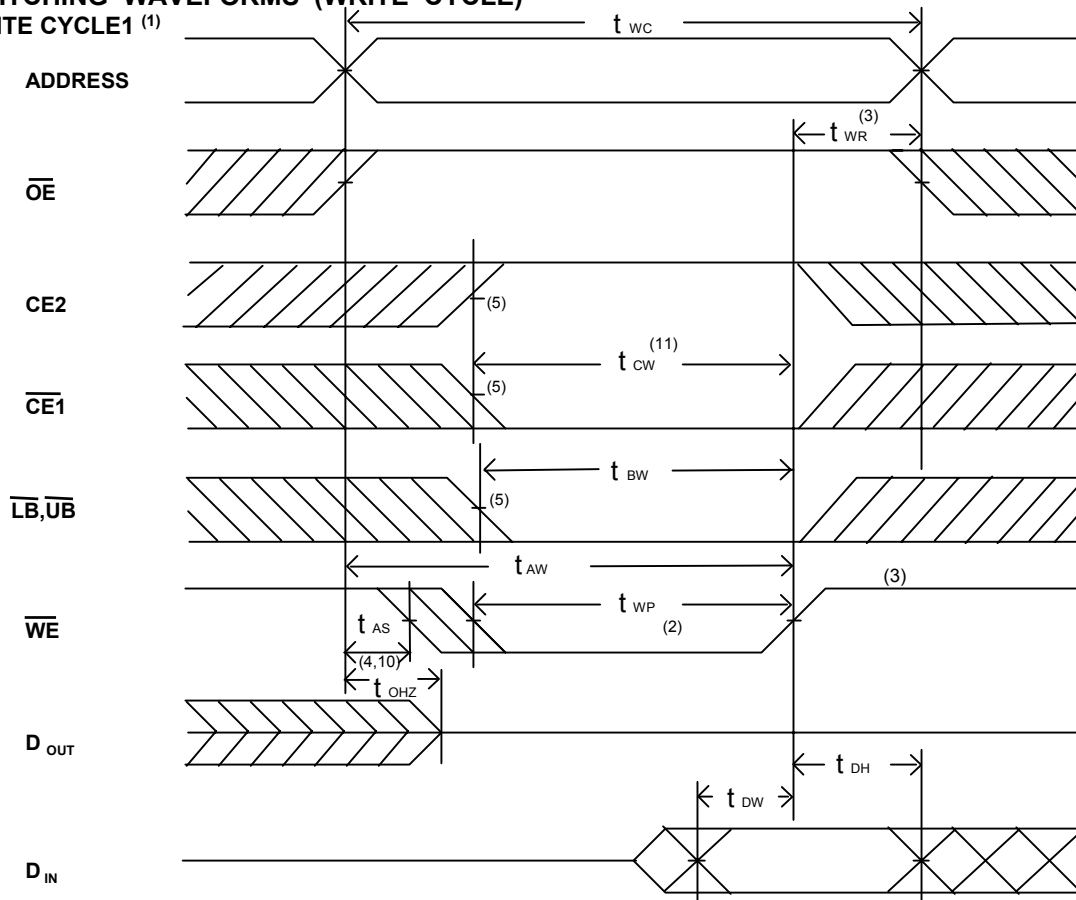
1.  $\overline{WE}$  is high in read Cycle.
2. Device is continuously selected when  $\overline{CE1} = V_{IL}$  and  $CE2 = V_{IH}$ .
3. Address valid prior to or coincident with CE transition low.
4.  $\overline{OE} = V_{IL}$ .
5. Transition is measured  $\pm 500\text{mV}$  from steady state with  $C_L = 5\text{pF}$  as shown in Figure 1B. The parameter is guaranteed but not 100% tested.

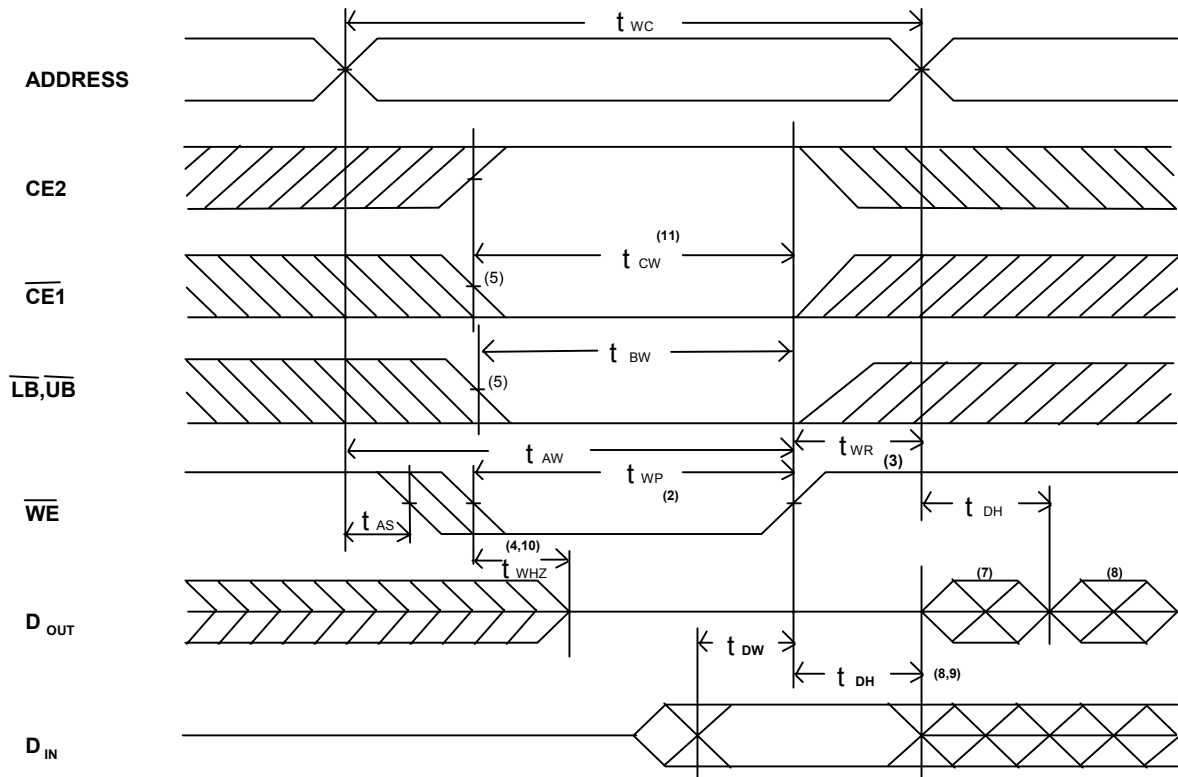
**AC ELECTRICAL CHARACTERISTICS ( TA = 0 to + 70°C, Vcc=5V)**
**WRITE CYCLE**

JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION	BS616LV8015-70			BS616LV8015-55			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
$t_{AVAX}$	$t_{WC}$	Write Cycle Time	70	--	--	55	--	--	ns
$t_{E1LWH}$	$t_{CW}$	Chip Select to End of Write	70	--	--	55	--	--	ns
$t_{AVWL}$	$t_{AS}$	Address Setup Time	0	--	--	0	--	--	ns
$t_{AVWH}$	$t_{AW}$	Address Valid to End of Write	70	--	--	55	--	--	ns
$t_{WLWH}$	$t_{WP}$	Write Pulse Width	35	--	--	30	--	--	ns
$t_{WHAX}$	$t_{WR}$	Write recovery Time (CE2, $\overline{CE1}$ , $\overline{WE}$ )	0	--	--	0	--	--	ns
$t_{BW}$	$t_{BW}^{(1)}$	Date Byte Control to End of Write ( $\overline{LB}$ , $\overline{UB}$ )	30	--	--	25	--	--	ns
$t_{WLQZ}$	$t_{WHZ}$	Write to Output in High Z	0	--	30	0	--	25	ns
$t_{DVWH}$	$t_{DW}$	Data to Write Time Overlap	30	--	--	25	--	--	ns
$t_{WHDX}$	$t_{DH}$	Data Hold from Write Time	0	--	--	0	--	--	ns
$t_{GHQZ}$	$t_{OHZ}$	Output Disable to Output in High Z	0	--	30	0	--	25	ns
$t_{WHOX}$	$t_{OW}$	End of Write to Output Active	5	--	--	5	--	--	ns

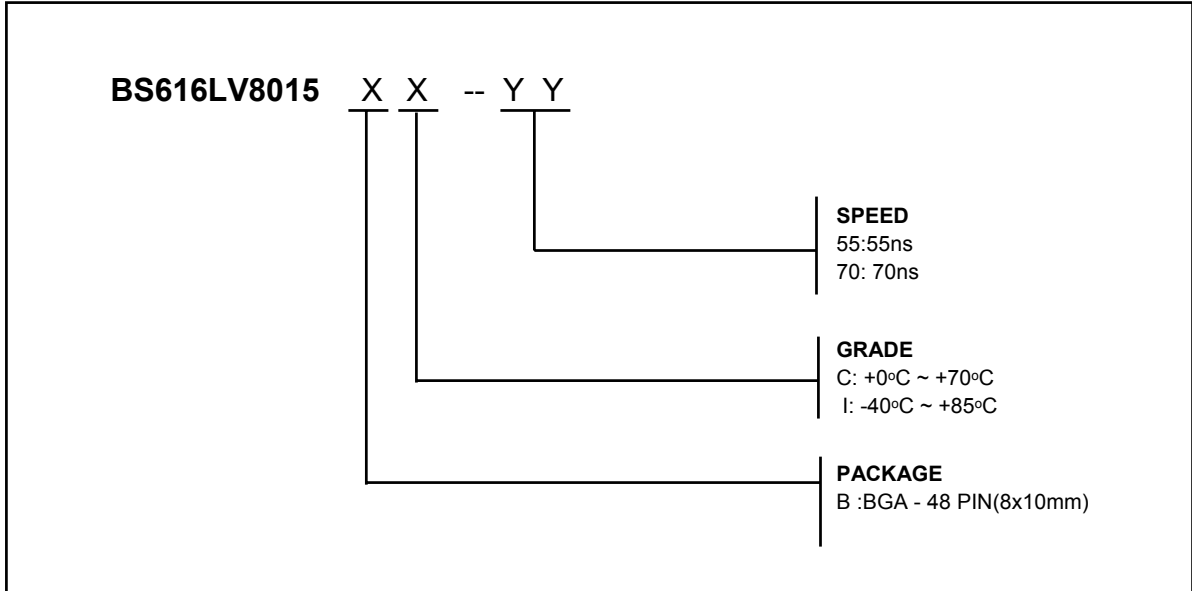
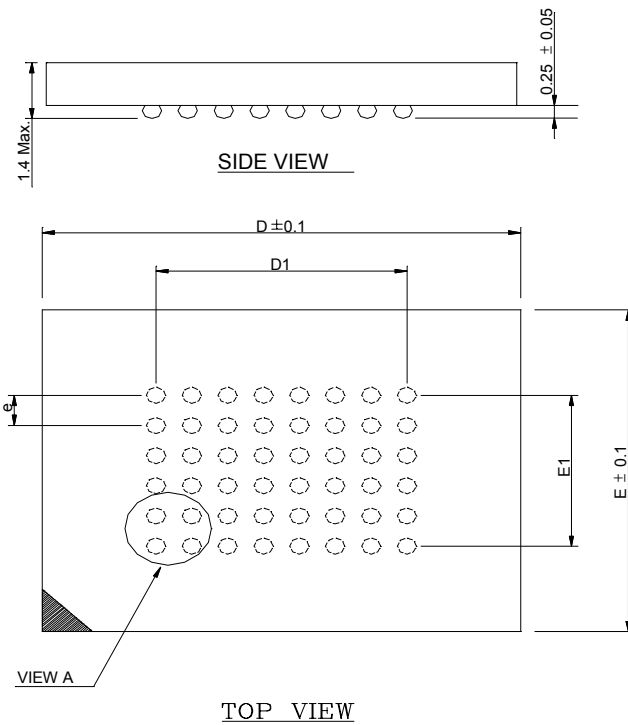
NOTE :

 1.  $t_{BW}$  is 30ns/25ns (@speed=70ns/55ns) with address toggle. ;  $t_{BW}$  is 70ns/55ns (@speed=70ns/55ns) without address toggle.

**SWITCHING WAVEFORMS (WRITE CYCLE)**
**WRITE CYCLE1<sup>(1)</sup>**


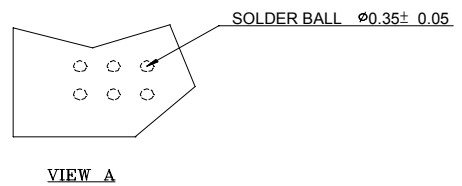
**WRITE CYCLE2 (1,6)**

**NOTES:**

1. WE must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of CE2, CE1 and WE low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3.  $t_{WR}$  is measured from the earlier of CE2 going low, or CE1 or WE going high at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the CE2 high transition or CE1 low transition occurs simultaneously with the WE low transitions or after the WE transition, output remain in a high impedance state.
6. OE is continuously low (OE =  $V_{IL}$ ).
7. DOUT is the same phase of write data of this write cycle.
8. DOUT is the read data of next address.
9. If CE2 is high or CE1 is low during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured  $\pm 500\text{mV}$  from steady state with  $C_L = 5\text{pF}$  as shown in Figure 1B. The parameter is guaranteed but not 100% tested.
11.  $t_{CW}$  is measured from the later of CE2 going high or CE1 going low to the end of write.

**■ ORDERING INFORMATION**

**■ PACKAGE DIMENSIONS**

**NOTES:**

- 1: CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
- 2: PIN#1 DOT MARKING BY LASER OR PAD PRINT.
- 3: SYMBOL "N" IS THE NUMBER OF SOLDER BALLS.

N	D	E	D1	E1	e
48	10.0	8.0	5.25	3.75	0.75



*48 mini-BGA (8 x 10mm)*



***REVISION HISTORY***

<b>Revision</b>	<b>Description</b>	<b>Date</b>	<b>Note</b>
<b>2.2</b>	<b>2001 Data Sheet release</b>	<b>Apr. 15, 2001</b>	
<b>2.3</b>	<b>Modify Standby Current (Typ. and Max.)</b>	<b>Jun. 29, 2001</b>	
<b>2.4</b>	<b>Modify some AC parameters. Modify 5V ICCSB1_Max(I-grade) from 50uA to 100uA.</b>	<b>April,11,2002</b>	