

FCD9N60NTM

N-Channel MOSFET

600V, 9A, 0.385mΩ

Features

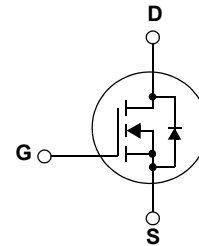
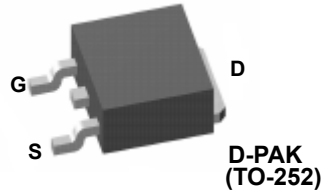
- $R_{DS(on)} = 0.330\Omega$ (Typ.) @ $V_{GS} = 10V, I_D = 4.5A$
- Ultra Low Gate Charge (Typ. Qg = 17.8nC)
- Low Effective Output Capacitance
- 100% Avalanche Tested
- RoHS Compliant



Description

The SupreMOS MOSFET, Fairchild's next generation of high voltage super-junction MOSFETs, employs a deep trench filling process that differentiates it from preceding multi-epi based technologies. By utilizing this advance technology and precise process control, SupreMOS provide world class Rsp, superior switching performance and ruggedness.

This SupreMOS MOSFET fits the industry's AC-DC SMPS requirements for PFC, server/telecom power, FPD TV power, ATX power, and industrial power applications.



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FCD9N60N	Units
V_{DSS}	Drain to Source Voltage	600	V
V_{GSS}	Gate to Source Voltage	± 30	V
I_D	Drain Current	-Continuous ($T_C = 25^\circ\text{C}$)	9.0
		-Continuous ($T_C = 100^\circ\text{C}$)	5.7
I_{DM}	Drain Current	- Pulsed (Note 1)	27
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	135
I_{AR}	Avalanche Current		9.0
E_{AR}	Repetitive Avalanche Energy		9.3
dv/dt	MOSFET dv/dt Ruggedness	100	V/ns
	Peak Diode Recovery dv/dt (Note 3)	15	
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	92.6
		- Derate above 25°C	0.74
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

*Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	FCD9N60N	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.35	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	62.5	

Package Marking and Ordering Information $T_C = 25^\circ\text{C}$ unless otherwise noted

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCD9N60N	FCD9N60NTM	D-PAK	380mm	16mm	2500

Electrical Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 1\text{mA}, V_{GS} = 0\text{V}, T_J = 25^\circ\text{C}$	600	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 1\text{mA}$, Referenced to 25°C	-	0.8	-	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 480\text{V}, V_{GS} = 0\text{V}$ $V_{DS} = 480\text{V}, V_{GS} = 0\text{V}, T_C = 125^\circ\text{C}$	-	-	10 100	μA
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 30\text{V}, V_{DS} = 0\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 4.5\text{A}$	-	0.330	0.385	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40\text{V}, I_D = 4.5\text{A}$	-	5.3	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 100\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	735	1000	pF
C_{oss}	Output Capacitance		-	40	53	pF
C_{rss}	Reverse Transfer Capacitance		-	3.5	5.5	pF
C_{oss}	Output Capacitance	$V_{DS} = 380\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	-	23.7	-	pF
$C_{oss\text{eff}}$	Effective Output Capacitance	$V_{DS} = 0\text{V to } 380\text{V}, V_{GS} = 0\text{V}$	-	122	-	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 380\text{V}, I_D = 4.5\text{A}$ $R_{GEN} = 4.7\Omega$	-	13.2	-	ns
t_r	Turn-On Rise Time		-	9.6	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	28.7	-	ns
t_f	Turn-Off Fall Time		(Note 4)	-	11.5	-
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 380\text{V}, I_D = 4.5\text{A}$ $V_{GS} = 10\text{V}$	-	17.8	-	nC
Q_{gs}	Gate to Source Gate Charge		-	4.2	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		(Note 4)	-	7.6	-
ESR	Equivalent Series Resistance(G-S)	Drain Open	-	2.65	-	Ω

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	9.0	-	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	27	-	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_{SD} = 9\text{A}$	-	-	1.2	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{V}, I_{SD} = 9\text{A}$	-	322	-	ns
Q_{rr}	Reverse Recovery Charge	$di_F/dt = 100\text{A}/\mu\text{s}$	-	5.04	-	μC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. $I_{AS} = 3\text{A}, R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 9\text{A}, di/dt \leq 200\text{A}/\mu\text{s}, V_{DD} \leq 380\text{V}$, Starting $T_J = 25^\circ\text{C}$
4. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

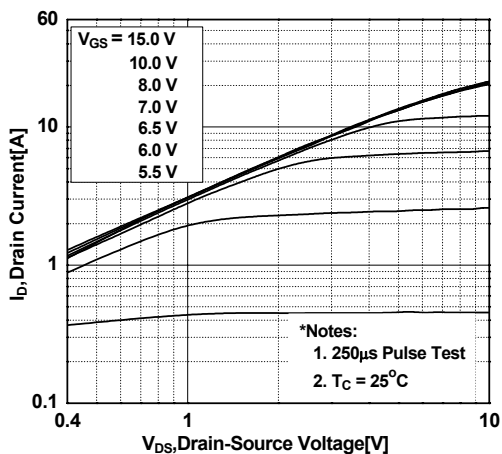


Figure 2. Transfer Characteristics

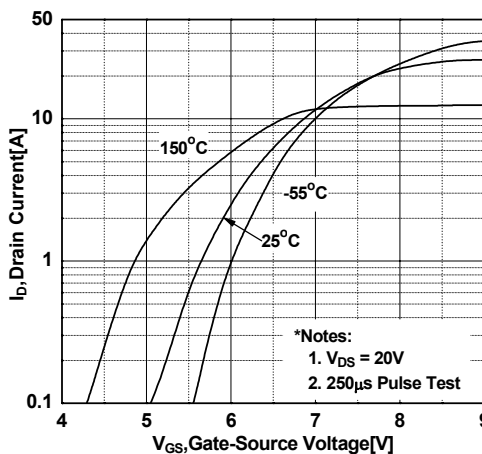


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

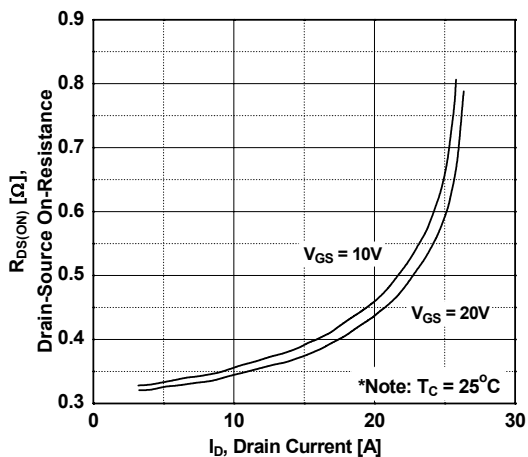


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

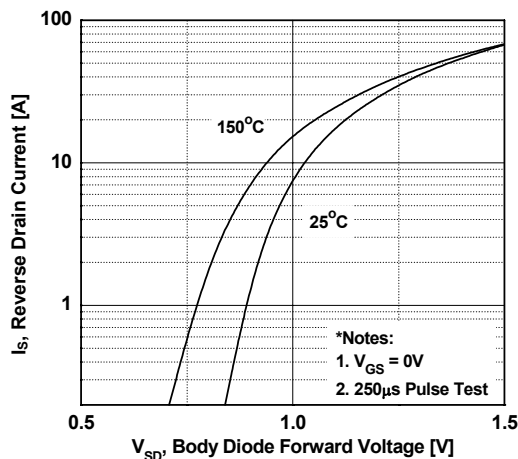


Figure 5. Capacitance Characteristics

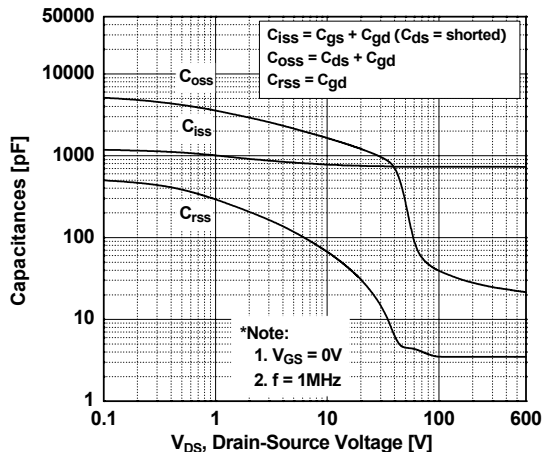
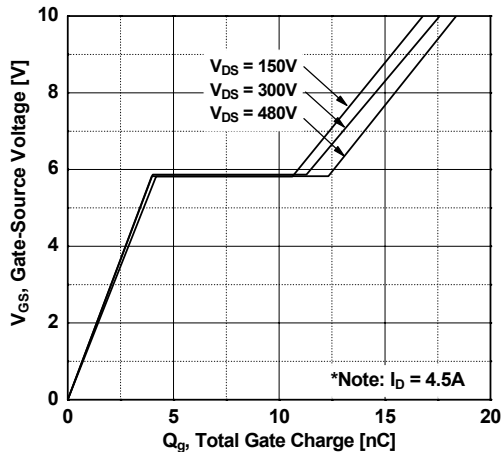


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

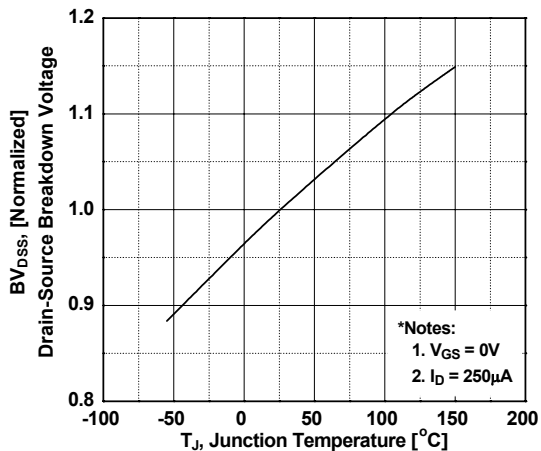


Figure 8. On-Resistance Variation vs. Temperature

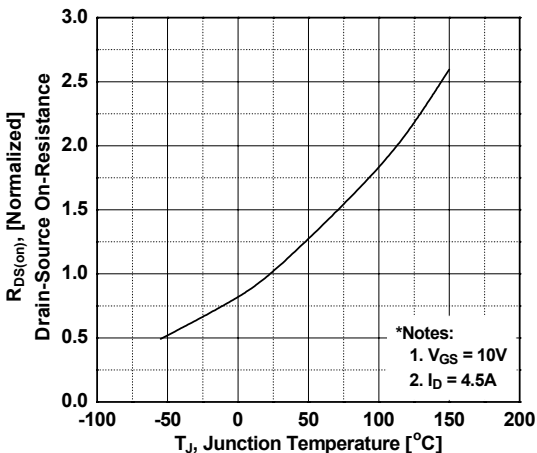


Figure 9. Maximum Safe Operating Area

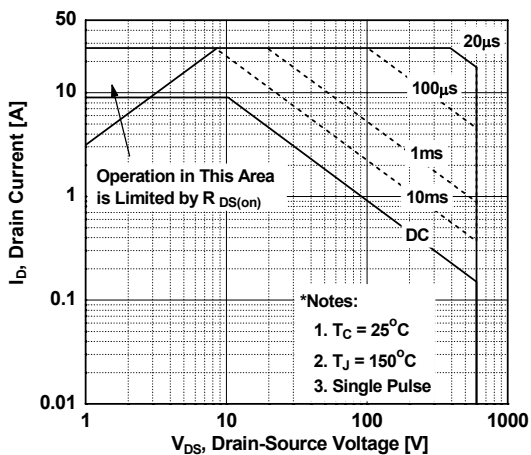


Figure 10. Maximum Drain Current vs. Case Temperature

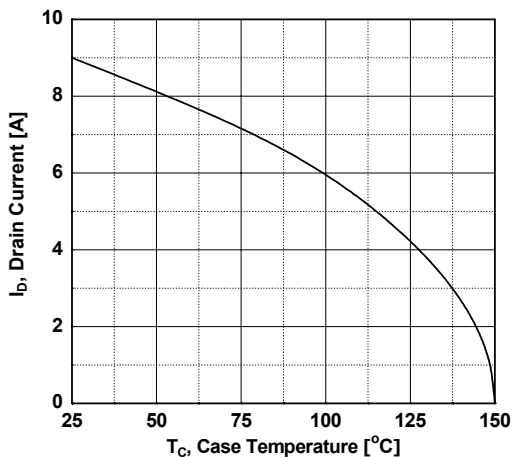
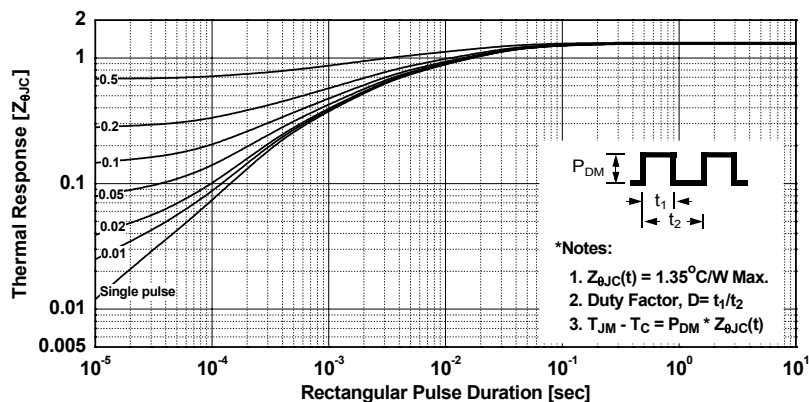
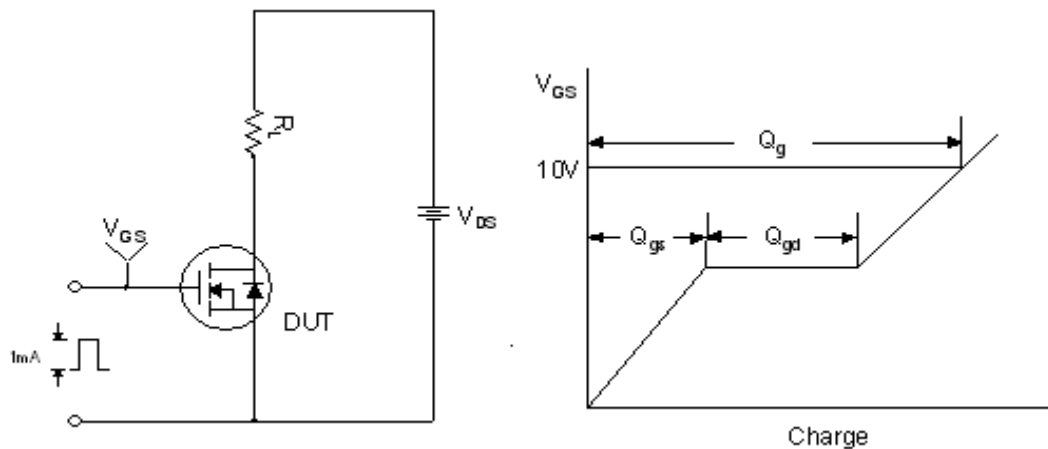


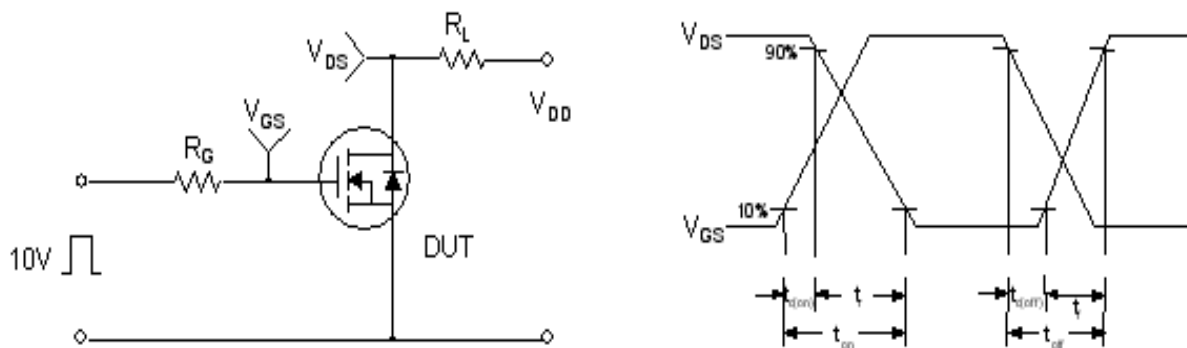
Figure 11. Transient Thermal Response Curve



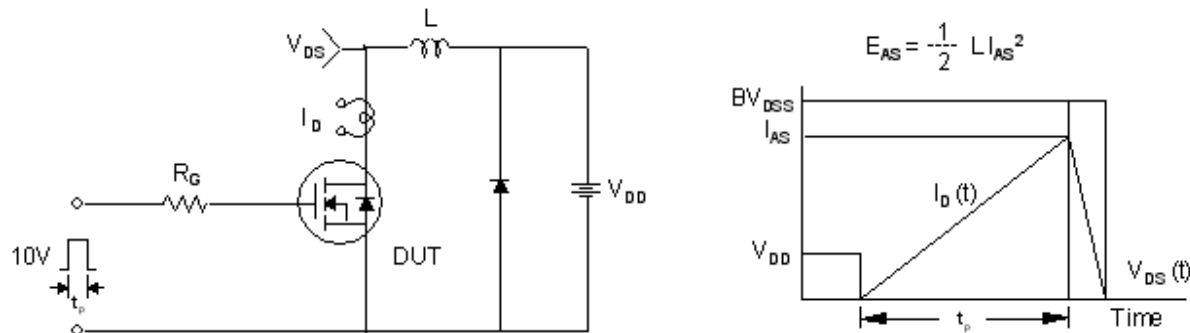
Gate Charge Test Circuit & Waveform



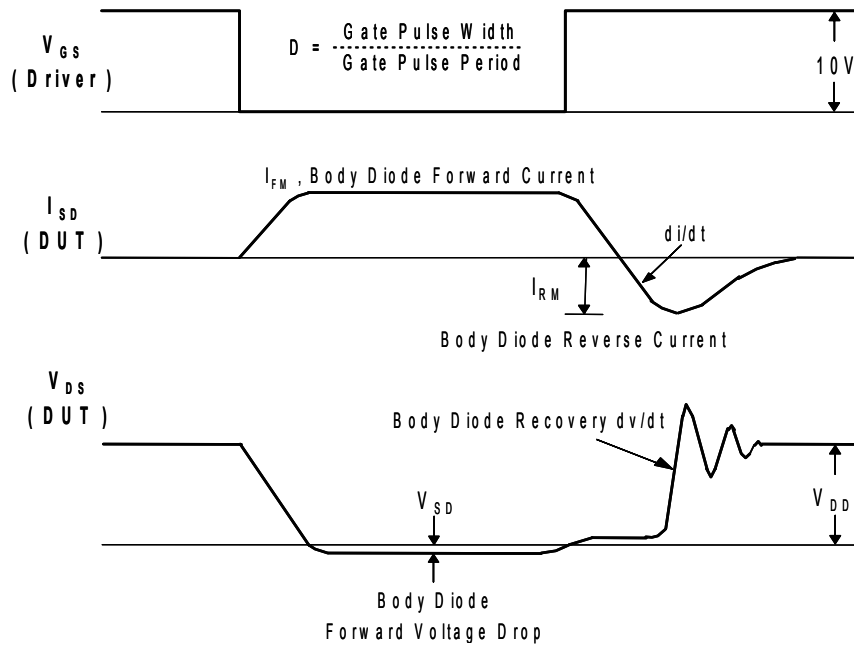
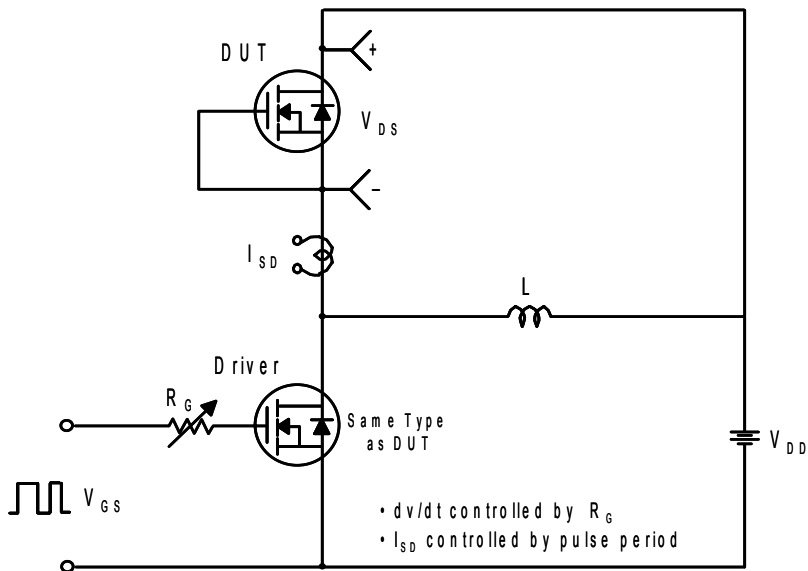
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

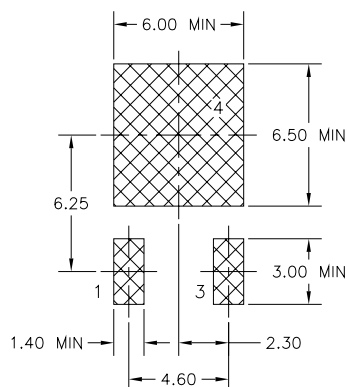
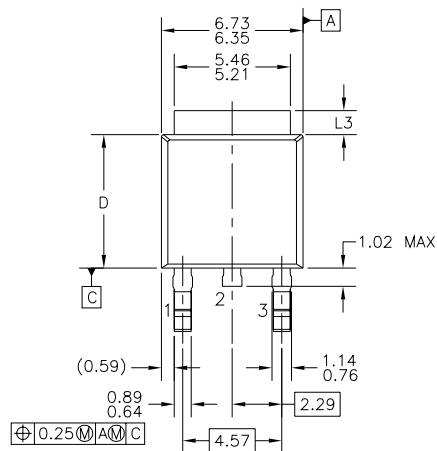


Peak Diode Recovery dv/dt Test Circuit & Waveforms

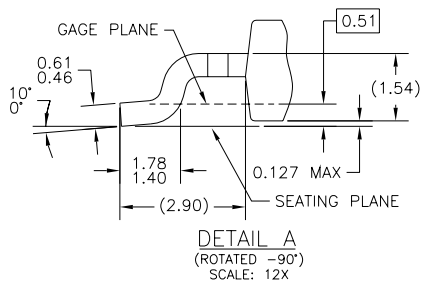
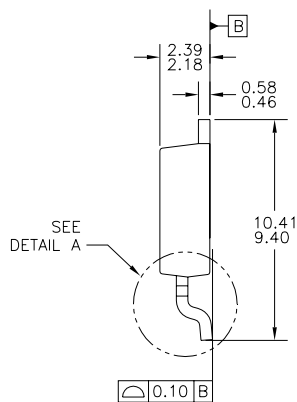
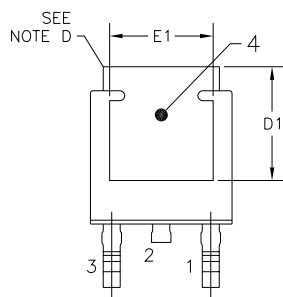


Mechanical Dimensions

D-PAK



LAND PATTERN RECOMMENDATION








- NOTES: UNLESS OTHERWISE SPECIFIED
- A) ALL DIMENSIONS ARE IN MILLIMETERS.
 - B) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA & AB, DATED NOV. 1999.
 - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
 - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
 - E) DIMENSIONS L3,D,E1&D1 TABLE:
- | | OPTION AA | OPTION AB |
|----|-----------|-----------|
| L3 | 0.89-1.27 | 1.52-2.03 |
| D | 5.97-6.22 | 5.33-5.59 |
| E1 | 4.32 MIN | 3.81 MIN |
| D1 | 5.21 MIN | 4.57 MIN |
- F) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.

Dimensions in Millimeters



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| CorePOWER™ | Gmax™ | QS™ | TinyBuck™ |
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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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