FAIRCHILD SEMICONDUCTOR®

September 2005

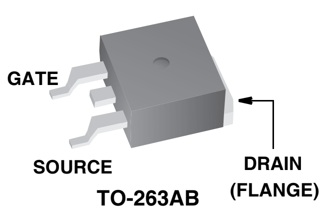
FDB5800
N-Channel Logic Level PowerTrench® MOSFET
60V, 80A, 7mΩ

Features

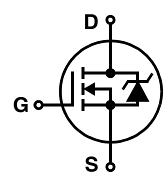
- $r_{DS(ON)}$ = 5.5mΩ (Typ.), V_{GS} = 5V, I_D = 80A
- High performance trench technology for extermely low Rdson
- Low Gate Charge
- High power and current handling capability
- Qualified to AEC Q101
- RoHS Compliant

Applications

- Motor/ Body Load Control
- ABS Systems
- Power Train Management
- Injection Systems
- DC-DC Converters and Off-Line UPS



TO-263AB
FDB SERIES



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	60	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current Continuous (T_C < 102°C, V_{GS} = 10V)	80	A
	Continuous (T_C < 90°C, V_{GS} = 5V)	80	A
	Continuous (T_{amb} = 25°C, V_{GS} = 10V, with $R_{\theta JA}$ = 43°C/W)	14	A
	Pulsed	Figure 4	A
E_{AS}	Single Pulse Avalanche Energy (Note 1)	652	mJ
P_D	Power dissipation	242	W
	Derate above 25°C	1.61	W/°C
T_J, T_{STG}	Operating and Storage Temperature	-55 to 175	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case TO-263	0.62	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-263 (Note 2)	62.5	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-263, 1in^2 copper pad area	43	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB5800	FDB5800	TO-263AB	330mm	24mm	800 units

Electrical Characteristics T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
B_{VDSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V	60	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 48V	-	-	1	μA
		V_{GS} = 0V, T_C = 150°C	-	-	250	
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V	-	-	±100	nA
On Characteristics						
$V_{GS(TH)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	1.0	-	2.5	V
$r_{DS(ON)}$	Drain to Source On Resistance	I_D = 80A, V_{GS} = 10V	-	4.6	6.0	mΩ
		I_D = 80A, V_{GS} = 4.5V	-	5.8	7.2	
		I_D = 80A, V_{GS} = 5V	-	5.5	7.0	
		I_D = 80A, V_{GS} = 10V, T_J = 175°C	-	10	12.6	
Dynamic Characteristics						
C_{ISS}	Input Capacitance	V_{DS} = 15V, V_{GS} = 0V, f = 1MHz	-	6625	-	pF
C_{OSS}	Output Capacitance		-	628	-	pF
C_{RSS}	Reverse Transfer Capacitance		-	262	-	pF
R_G	Gate Resistance	V_{GS} = 0.5V, f = 1MHz	-	1.4	-	Ω
$Q_{g(TOT)}$	Total Gate Charge at 10V	V_{GS} = 0V to 10V; V_{DD} = 30V, I_D = 80A, I_g = 1.0mA	-	104	135	nC
$Q_{g(5)}$	Total Gate Charge at 5V	V_{GS} = 0V to 5V	-	55	72	nC
$Q_{g(TH)}$	Threshold Gate Charge	V_{GS} = 0V to 1V	-	6.0	-	nC
Q_{gs}	Gate to Source Gate Charge		-	18.4	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau		-	12.5	-	nC
Q_{gd}	Gate to Drain “Miller” Charge		-	20.1	-	nC

Switching Characteristics (V_{GS} = 5V)

t_{ON}	Turn-On Time	V_{DD} = 30V, I_D = 80A V_{GS} = 5V, R_{GS} = 2Ω	-	-	62.1	ns
$t_{d(ON)}$	Turn-On Delay Time		-	20.3	-	ns
t_r	Rise Time		-	22.0	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	27.1	-	ns
t_f	Fall Time		-	12.1	-	ns
t_{OFF}	Turn-Off Time		-	-	59.0	ns

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Voltage	I_{SD} = 80A	-	-	1.25	V
		I_{SD} = 40A	-	-	1.0	V
t_{rr}	Reverse Recovery Time	I_{SD} = 60A, dI_{SD}/dt = 100A/µs	-	-	44	ns
Q_{RR}	Reverse Recovered Charge	I_{SD} = 60A, dI_{SD}/dt = 100A/µs	-	-	57	nC

Notes:
1: Starting T_J = 25°C, L = 1mH, I_{AS} = 36A, V_{DD} = 54V, V_{GS} = 10V.
2: Pulse width = 100s.

This product has been designed to meet the extreme test conditions and environment demanded by the automotive industry. For a copy of the requirements, see AEC Q101 at: http://www.aecouncil.com/
All Fairchild Semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

Typical Characteristics $T_C = 25°C$ unless otherwise noted

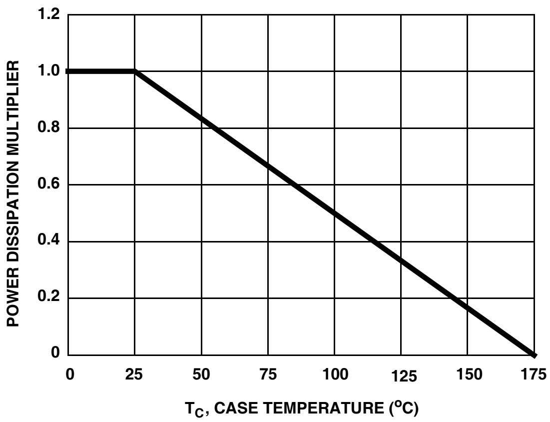


Figure 1. Normalized Power Dissipation vs Case Temperature

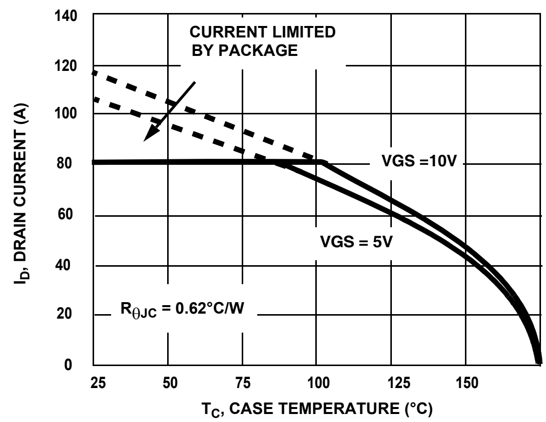


Figure 2. Maximum Continuous Drain Current vs Case Temperature

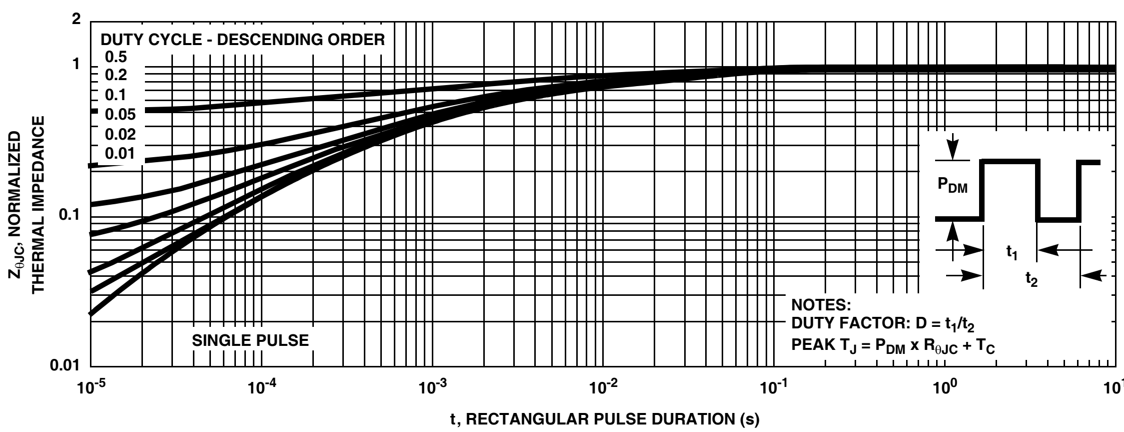


Figure 3. Normalized Maximum Transient Thermal Impedance

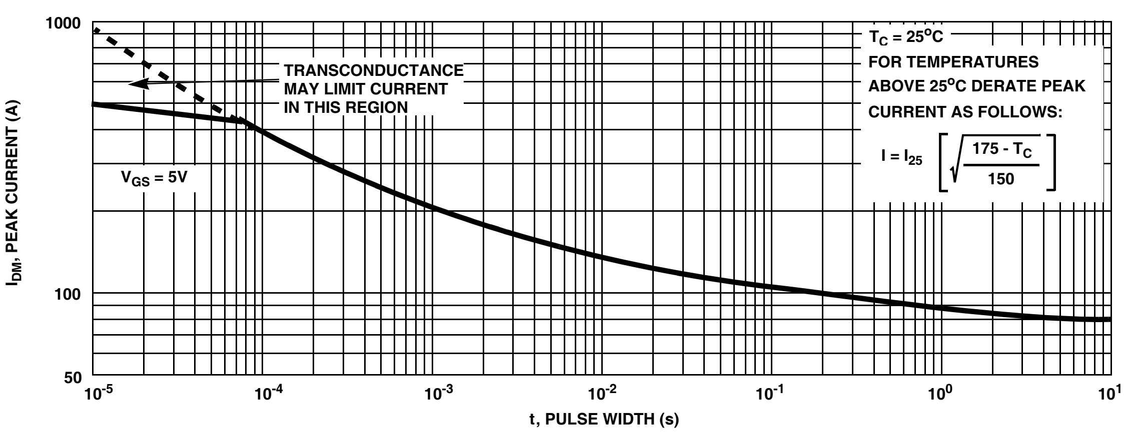


Figure 4. Peak Current Capability

Typical Characteristics T_C = 25°C unless otherwise noted

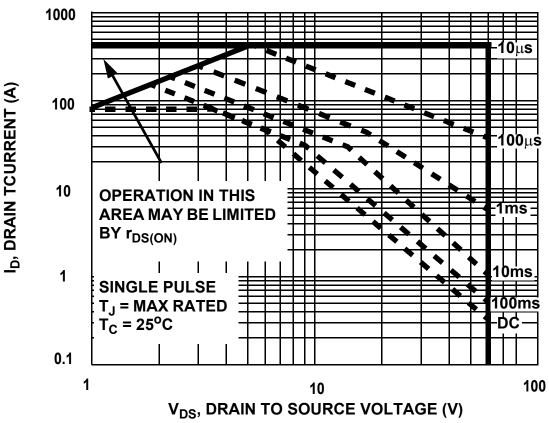
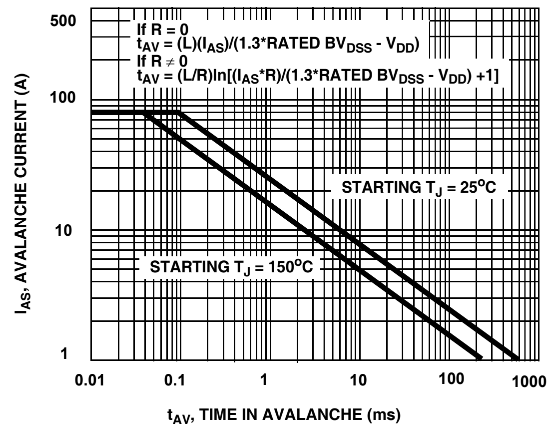


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

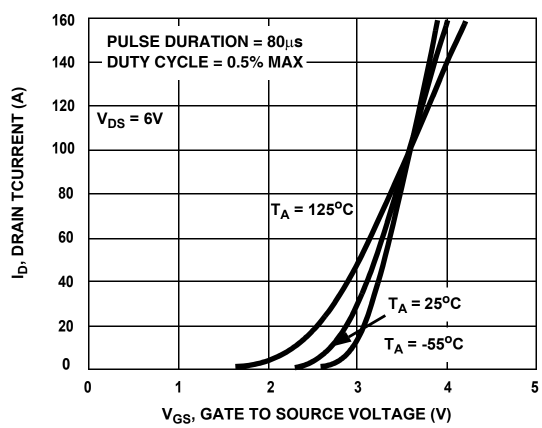


Figure 7. Transfer Characteristics

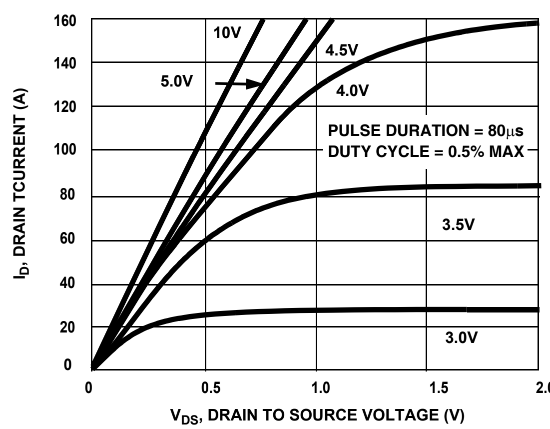


Figure 8. Saturation Characteristics

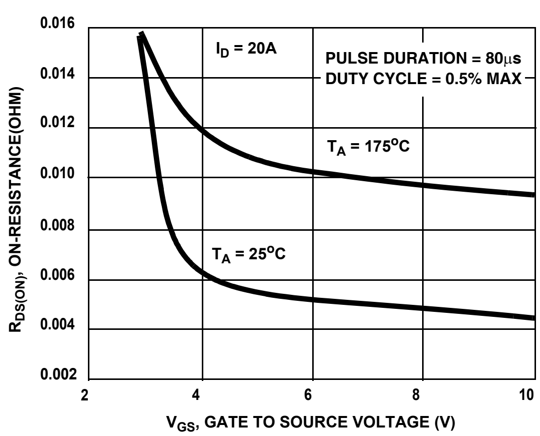


Figure 9. On-Resistance Variation vs Gate-to-Source Voltage

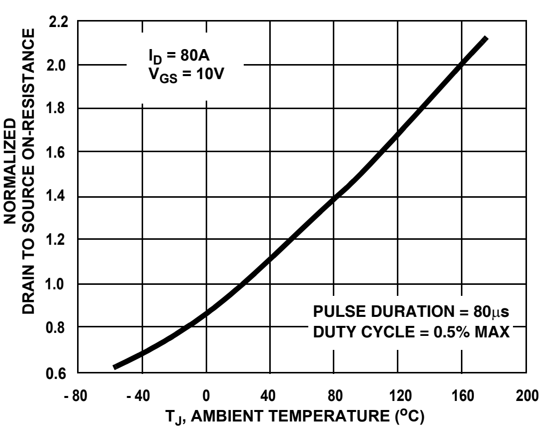


Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

Typical Characteristics T_C = 25°C unless otherwise noted

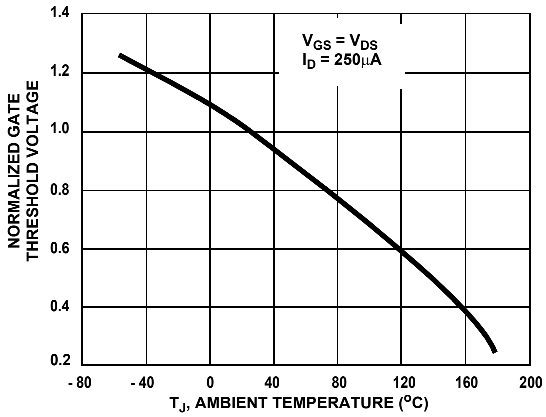


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

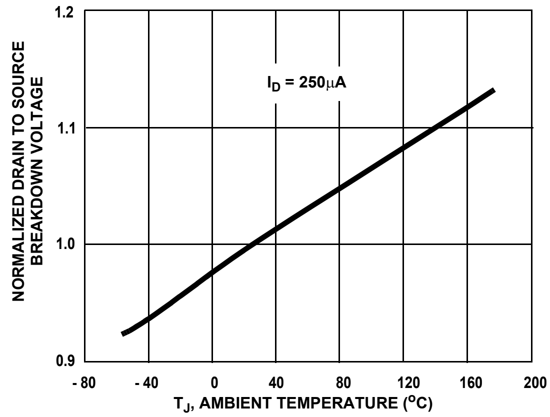


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

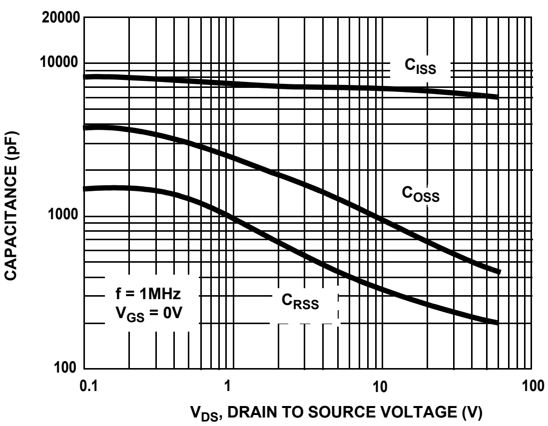


Figure 13. Capacitance vs Drain to Source Voltage

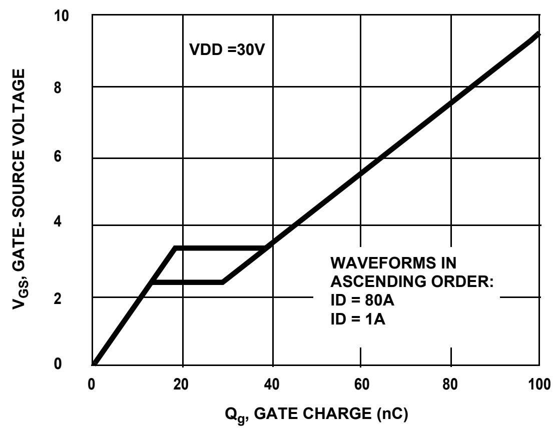


Figure 14. Gate Charge Waveforms for Constant Gate Current

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