240pin DDR2 VLP Registerd DIMMs based on 1Gb C version

This Hynix DDR2 VLP(Very Low Profile) registered Dual In-Line Memory Module (DIMM) series consists of 1Gb C version DDR2 SDRAMs in Fine Ball Grid Array(FBGA) packages on a 240pin glass-epoxy substrate. This Hynix 1Gb C version based VLP Registered DIMM series provide a high performance 8 byte interface in 133.35mm width form factor of industry standard. It is suitable for easy interchange and addition.

ORDERING INFORMATION

Part Name	Density	Org.	Component Configuration	Ranks	Parity Support
HYMP112P72CP8L-C4/Y5/S6	1GB	128Mbx72	128Mbx8(HY5PS1G821CFP)*9	1	O
HYMP125P72CP4L-C4/Y5/S6	2GB	256Mbx72	256Mbx4(HY5PS1G421CFP)*18	1	O
HYMP351P72CMP4L-C4/Y5/S6	4GB	512Mbx72	512Mbx4(HY5PS2G421CMP)*18	2	O
HYMP41GP72CNP4L-C4/Y5	8GB	1Gbx72	1Gbx4(HY5PS4G421CNP)*18	4	O

Note:
1. “P” of part number[12th digit] stands for Lead free products.

SPEED GRADE & KEY PARAMETERS

	C4 (DDR2-533)	Y5 (DDR2-667)	S6 (DDR2-800)	Unit
Speed@CL3	400	400	-	Mbps
Speed@CL4	533	533	400	Mbps
Speed@CL5	-	667	533	Mbps
Speed@CL6	-	-	800	Mbps
CL-tRCD-tRP	4-4-4	5-5-5	6-6-6	tCK

FEATURES

- JEDEC standard 1.8V +/- 0.1V Power Supply
- V_{DDQ} : 1.8V +/- 0.1V
- All inputs and outputs are compatible with SSTL_1.8 interface
- 4 Bank architecture
- Posted $\overline{CAS}$
- Programmable CAS Latency 3 , 4 , 5
- OCD (Off-Chip Driver Impedance Adjustment)
- ODT (On-Die Termination)
- Fully differential clock operations (CK & $\overline{CK}$)
- Programmable Burst Length 4 / 8 with both sequential and interleave mode
- Average Auto Refresh Period 7.8us under T_{CASE} 85℃, 3.9us at 85℃ < T_{CASE} ≤ 95 ℃
- High Temperature Self-Refresh Entry enablble features
- PASR(Partial Array Self- Refresh)
- 8192 refresh cycles / 64ms
- Serial presence detect with EEPROM
- DDR2 SDRAM Package: 60ball FBGA
- 133.35 x 18.29 mm form factor
- Lead-free Products are RoHS compliant

ADDRESS TABLE

Density	Organization	Ranks	SDRAMs	# of DRAMs	# of row/bank/column Address	Refresh Method
1GB	128Mb x 72	1	128Mb x 8	9	14(A0~A13)/3(BA0~BA2)/10(A0~A9)	8K / 64ms
2GB	256Mb x 72	1	256Mb x 4	18	14(A0~A13)/3(BA0~BA2)/11(A0~A9,A11)	8K / 64ms
4GB	512Mb x 72	2	256Mb x 4	36	14(A0~A13)/3(BA0~BA2)/11(A0~A9,A11)	8K / 64m
8GB	1Gb x 72	4	256Mb x 4	72	14(A0~A13)/3(BA0~BA2)/11(A0~A9,A11)	8K / 64m

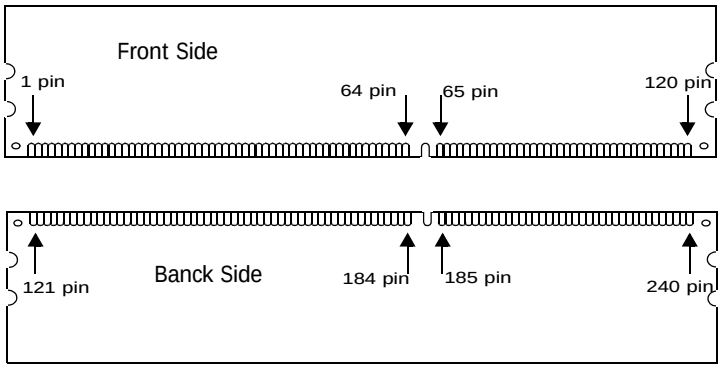
Input/Output Functional Description

Symbol	Type	Polarity	Pin Description
CK0	IN	Positive Edge	Positive line of the differential pair of system clock inputs that drives input to the on-DIMM PLL.
$\overline{CK0}$	IN	Negative Edge	Negative line of the differential pair of system clock inputs that drives input to the on-DIMM PLL.
CKE[1:0]	IN	Active High	Activates the DDR2 SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode or the Self Refresh mode.
$\overline{S}$[1:0]	IN	Active Low	Enables the associated DDR2 SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Rank 0 is selected by $\overline{S}$0; Rank 1 is selected by $\overline{S}$1
ODT[1:0]	IN	Active High	On-Die Termination signals.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	IN	Active Low	When sampled at the positive rising edge of the clock. $\overline{RAS}$,$\overline{CAS}$ and $\overline{WE}$(ALONG WITH S) define the command being entered.
Vref	Supply		Reference voltage for SSTL18 inputs
V_{DDQ}	Supply		Power supplies for the DDR2 SDRAM output buffers to provide improved noise immunity. For all current DDR2 unbuffered DIMM designs, V_{DDQ} shares the same power plane as V_{DD} pins.
BA[1:0]	IN	-	Selects which DDR2 SDRAM internal bank of four is activated.
A[9:0], A10/AP A[13:11]	IN	-	During a Bank Activate command cycle, Address input defines the row address(RA0~RA13) During a Read or Write command cycle, Address input defines the column address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high., autoprecharge is selected and BA0-BAn defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle., AP is used in conjunction with BA0-BAn to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0-BAn inputs. If AP is low, then BA0-BAn are used to define which bank to precharge.
DQ[63:0], CB[7:0]	IN	-	Data and Check Bit Input/Output pins.
DM[8:0]	IN	Active High	DM is an input mask signal for write data. Input data is masked when DM is sampled High coincident with that input data during a write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
V_{DD},V_{SS}	Supply		Power and ground for the DDR2 SDRAM input buffers, and core logic. V_{DD} and V_{DDQ} pins are tied to V_{DD}/V_{DDQ} planes on these modules.
DQS[17:0]	I/O	Positive Edge	Positive line of the differential data strobe for input and output data
$\overline{DQS}$[17:0]	I/O	Negative Edge	Negative line of the differential data strobe for input and output data
SA[2:0]	IN	-	These signals are tied at the system planar to either V_{SS} or V_{DDSPD} to configure the serial SPD EEPROM address range.
SDA	I/O	-	This is a bidirectional pin used to transfer data into or out of the SPD EEPROM. A resister may be connected from the SDA bus line to V_{DDSPD} on the system planar to act as a pull up.
SCL	IN	-	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from SCL to V_{DDSPD} to act as a pull up on the system board.
VDDSPD	Supply		Power supply for SPD EEPROM. This supply is separate from the VDD/VDDQ power plane. EEPROM supply is operable from 1.7V to 3.6V.
RESET	IN		The RESET pin is connected to the RST pin on the register and to the OE pin on the PLL. When low, all register outputs will be driven low and the PLL clocks to the DRAMs and register(s) will be set to low level (the PLL will remain synchronized with the input clock)
Par_In	IN		Parity bit for the Address and Control bus(“1”. Odd, “0”.Even)
Err_Out	OUT		Parity error found in the Address and Control bus
TEST			Used by memory bus analysis tools(unused on memory DIMMs)

PIN DESCRIPTION

Pin	Pin Description	Pin	Pin Description
CK0	Clock Input,positive line	ODT[1:0]	On Die Termination Inputs
$\overline{CK0}$	Clock input,negative line	VDDQ	DQs Power Supply
CKE0~CKE1	Clock Enable Input	DQ0~DQ63	Data Input/Output
$\overline{RAS}$	Row Address Strobe	CB0~CB7	Data check bits Input/Output
$\overline{CAS}$	Column Address Strobe	DQS(0~8)	Data strobes
$\overline{WE}$	Write Enable	$\overline{DQS}$(0~8)	Data strobes,negative line
$\overline{S}$0,$\overline{S}$1	Chip Select Input	DM(0~8), DQS(9~17)	Data Maskes/Data strobes
A0~A9, A11~A13	Address input	$\overline{DQS}$(9~17)	Data strobes,negative line
A10/AP	Address input/Autoprecharge	RFU	Reserved for Future Use
BA0,BA1	SDRAM Bank Address	NC	No Connect
SCL	Serial Presence Detect(SPD) Clock Input	TEST	Memory bus test tool (Not Connected and Not Usable on DIMMs)
SDA	SPD Data Input/Output	VDD	Core Power
SA0~SA2	E^2PROM Address Inputs	VDDQ	I/O Power
Par_In	Parity bit for the Address and Control bus	VSS	Ground
$\overline{Err\_Out}$	Parity error found on the Address	VREF	Input/Output Reference
$\overline{RESET}$	Reset Enable	VDDSPD	SPD Power
CB0~CB7	Data Check bit Inputs/Outputs		

PIN LOCATION



PIN ASSIGNMENT

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VREF	41	VSS	81	DQ33	121	VSS	161	CB4	201	VSS
2	VSS	42	CB0	82	VSS	122	DQ4	162	CB5	202	DM4/DQS13
3	DQ0	43	CB1	83	$\overline{DQS}$4	123	DQ5	163	VSS	203	$\overline{DQS}$13
4	DQ1	44	VSS	84	DQS4	124	VSS	164	DM8,DQS17	204	VSS
5	VSS	45	$\overline{DQS}$8	85	VSS	125	DM0/DQS9	165	$\overline{DQS}$17	205	DQ38
6	$\overline{DQS}$0	46	DQS8	86	DQ34	126	$\overline{DQS}$9	166	VSS	206	DQ39
7	DQS0	47	VSS	87	DQ35	127	VSS	167	CB6	207	VSS
8	VSS	48	CB2	88	VSS	128	DQ6	168	CB7	208	DQ44
9	DQ2	49	CB3	89	DQ40	129	DQ7	169	VSS	209	DQ45
10	DQ3	50	VSS	90	DQ41	130	VSS	170	VDDQ	210	VSS
11	VSS	51	VDDQ	91	VSS	131	DQ12	171	NC,CKE1	211	DM5/DQS14
12	DQ8	52	CKE0	92	$\overline{DQS}$5	132	DQ13	172	VDD	212	$\overline{DQS}$14
13	DQ9	53	VDD	93	DQS5	133	VSS	173	A15,NC	213	VSS
14	VSS	54	BA2,NC	94	VSS	134	DM1/DQS10	174	A14,NC	214	DQ46
15	$\overline{DQS}$1	55	NC,$\overline{Err_Out}$	95	DQ42	135	$\overline{DQS}$10	175	VDDQ	215	DQ47
16	DQS1	56	VDDQ	96	DQ43	136	VSS	176	A12	216	VSS
17	VSS	57	A11	97	VSS	137	RFU	177	A9	217	DQ52
18	$\overline{RESET}$	58	A7	98	DQ48	138	RFU	178	VDD	218	DQ53
19	NC	59	VDD	99	DQ49	139	$\overline{VSS}$	179	A8	219	VSS
20	VSS	60	A5	100	VSS	140	DQ14	180	A6	220	RFU
21	DQ10	61	A4	101	SA2	141	DQ15	181	VDDQ	221	RFU
22	DQ11	62	VDDQ	102	NC(TEST)	142	VSS	182	A3	222	VSS
23	VSS	63	A2	103	VSS	143	DQ20	183	A1	223	DM6/DQS15
24	DQ16	64	VDD	104	$\overline{DQS}$6	144	DQ21	184	VDD	224	NC,$\overline{DQS}$15
25	DQ17	Key		105	DQS6	145	VSS	Key		225	VSS
26	VSS	65	VSS	106	VSS	146	DM2/DQS11	185	CK0	226	DQ54
27	$\overline{DQS}$2	66	VSS	107	DQ50	147	$\overline{DQS}$11	186	$\overline{CK0}$	227	DQ55
28	DQS2	67	VDD	108	DQ51	148	VSS	187	VDD	228	VSS
29	VSS	68	NC,$\overline{Err\_Out}$	109	VSS	149	DQ22	188	A0	229	DQ60
30	DQ18	69	VDD	110	DQ56	150	DQ23	189	VDD	230	DQ61
31	DQ19	70	A10/AP	111	DQ57	151	VSS	190	BA1	231	VSS
32	VSS	71	BA0	112	VSS	152	DQ28	191	VDDQ	232	DM7/DQS16
33	DQ24	72	VDDQ	113	$\overline{DQS}$7	153	DQ29	192	$\overline{RAS}$	233	NC,$\overline{DQS}$16
34	DQ25	73	$\overline{WE}$	114	DQS7	154	VSS	193	$\overline{S}$0	234	VSS
35	VSS	74	$\overline{CAS}$	115	VSS	155	DM3/DQS12	194	VDDQ	235	DQ62
36	$\overline{DQS}$3	75	VDDQ	116	DQ58	156	$\overline{DQS}$12	195	ODT0	236	DQ63
37	DQS3	76	NC, $\overline{S}$1	117	DQ59	157	VSS	196	A13,NC	237	VSS
38	VSS	77	NC, ODT1	118	VSS	158	DQ30	197	VDD	238	VDDSPD
39	DQ26	78	VDDQ	119	SDA	159	DQ31	198	VSS	239	SA0
40	DQ27	79	VSS	120	SCL	160	VSS	199	DQ36	240	SA1
		80	DQ32					200	DQ37		

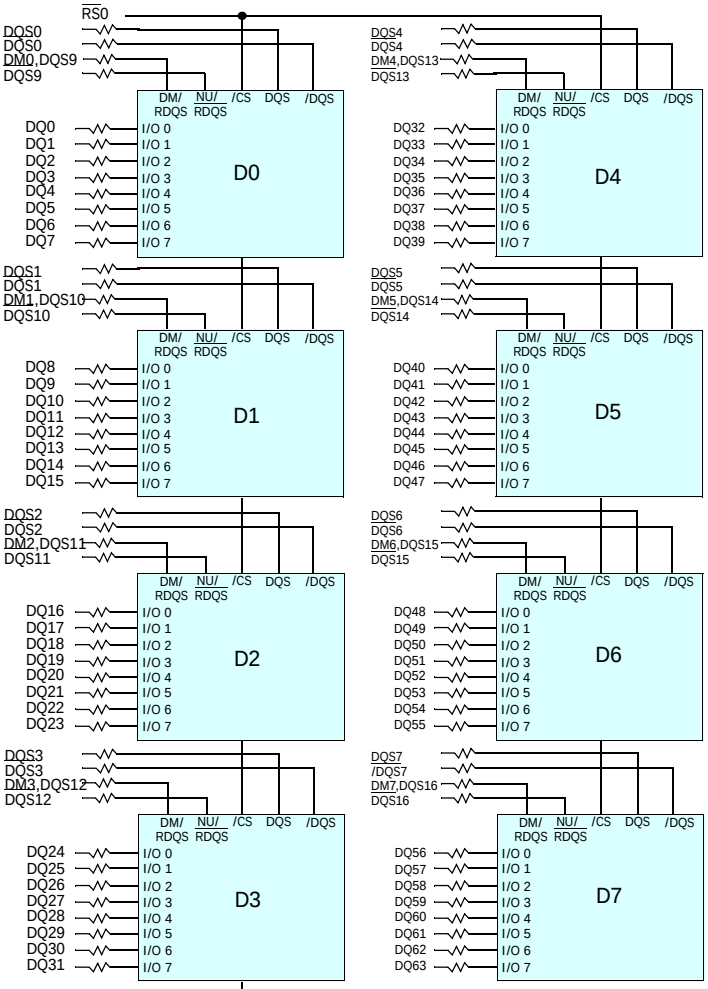
NC= No Connect, RFU= Reserved for Future Use.

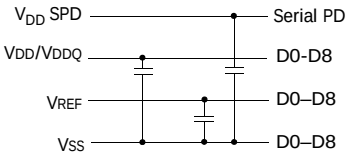
Note:

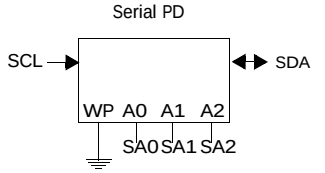
1. RESET(Pin 18) is connected to both OE of PLL and Reset of register.
2. NC/Err_out (Pin 55) and NC/Par_In(Pin68) are for optional function to check address and command parity.
3. The Test pin(Pin 102) is reserved for bus analysis probes and is not connected on normal memory modules(DIMMs)

FUNCTIONAL BLOCK DIAGRAM

1GB(128Mbx72) : HYMP112P72CP8L

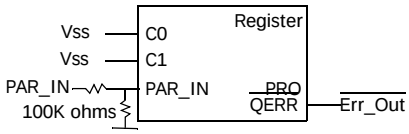




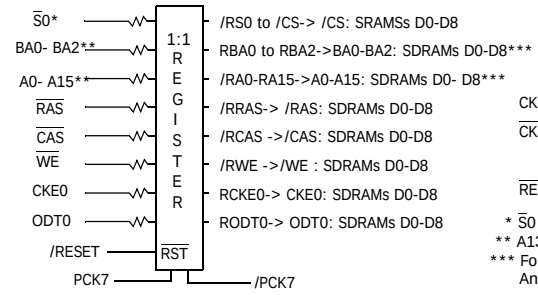


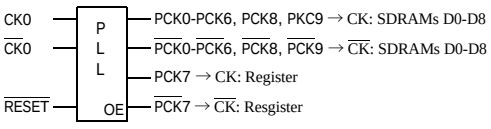
Note:
1.DQ-to-I/O wiring may be changed within a byte.
2.Unless otherwise noted, resistor values are 22 Ohms +/-5%.

Signals for Address and Command Parity Function (Raw Card F, F and AC)



The resistors on Par_In, A13, A14, A15, BA2 and the signal line of Err_Out refer to the section:
"Register Options for unused Address inputs"

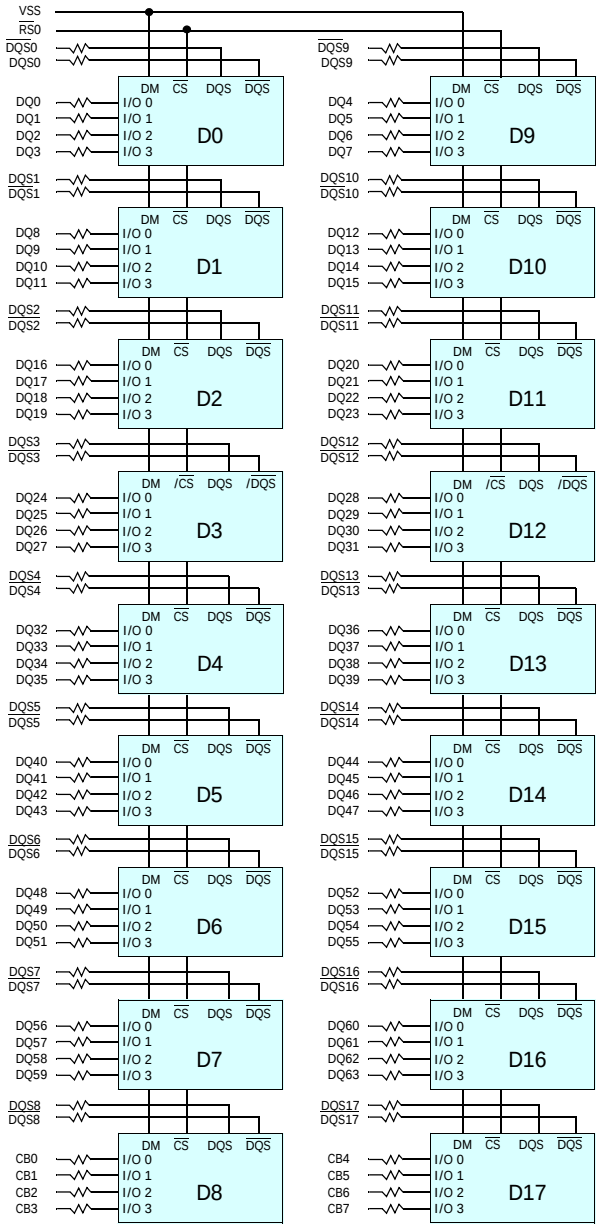


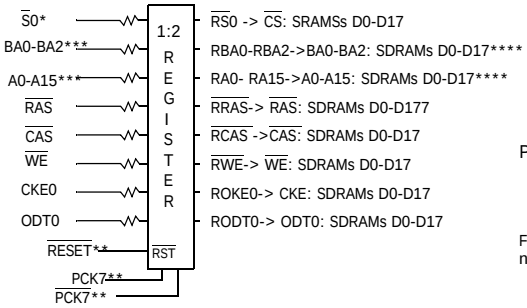


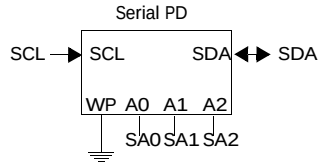
* S0 connects to DCS and VDD connects to CSR on the register. S1, CKE1 and ODT1 are NC
** A13-15, BA2 have the optional pull down resistors(100K ohms), which is not indicated here.
*** For Rqw Card R and A Co, post register A14, A15 and BA2 are not connected to the SDRAMs. And for Raw Card AC1, post register A14 and A15 are not connected to the SDRAMs.

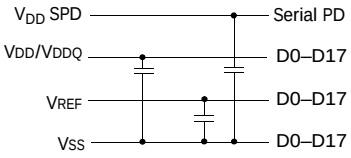
FUNCTIONAL BLOCK DIAGRAM

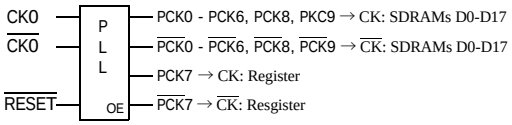
2GB(256Mbx72) : HYMP125P72CP4L











Note:
1. DQ-to-I/O wiring may be changed within a byte.
2. Unless otherwise noted, resistor values are 22 Ohms +/-5%.

* S0 connects to DCS or Register A and CSR of Register B.
CSR of Register A and DCS of Register B connects to VDD.

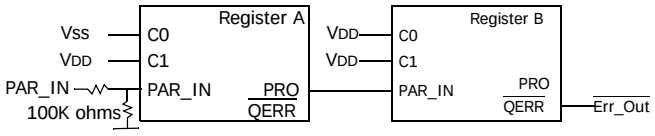
** RESET, PCK7 and PCK7 connects to both Registers.
Other signals connects to one of two Registers.
Raw Card V has only one register.

*** A13-A15, BA2 have the optional pull down resistors (100K ohms), which is not indicated here.

**** For /raw /card U0 and V, post register A14, A15 and BA2 are not connected to the SDRAMs.
And for Raw Care U1, post register A14 and A15 are not connected to the SDRAMs.

The resistors on Par_In, A13, A14, A15, BA2 and the signal line of Err_Out refer to the section:
"Register Options for unused Address inputs"

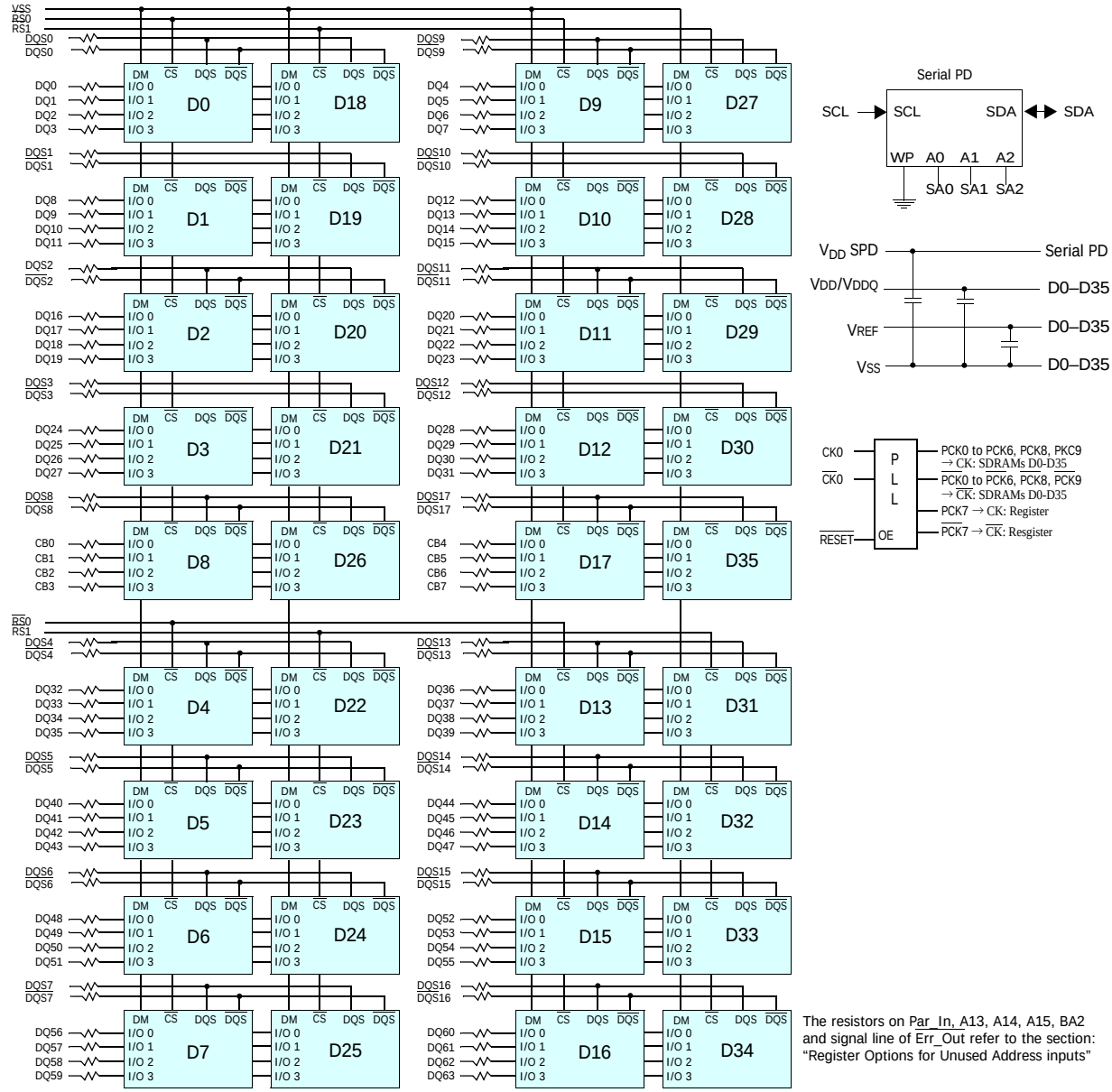
Signals for Address and Command Parity Function (Raw Card H, U)



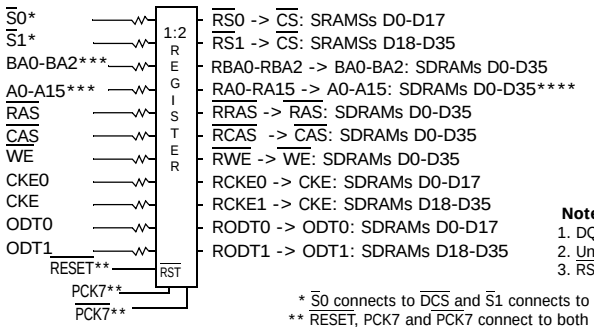
For R/C U, 0 ohm resistor is placed at the end of Err_Out just before the edge connector and is not populated for the non-parity card.

FUNCTIONAL BLOCK DIAGRAM

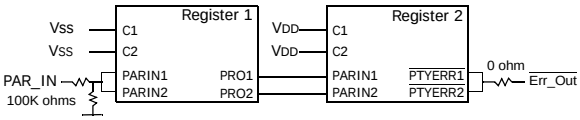
4GB(256Mbx72) : HYMP351P72CMP4L



The resistors on Par_In, A13, A14, A15, BA2 and signal line of Err_Out refer to the section: "Register Options for Unused Address inputs"



Signals for Address and Command Parity Function



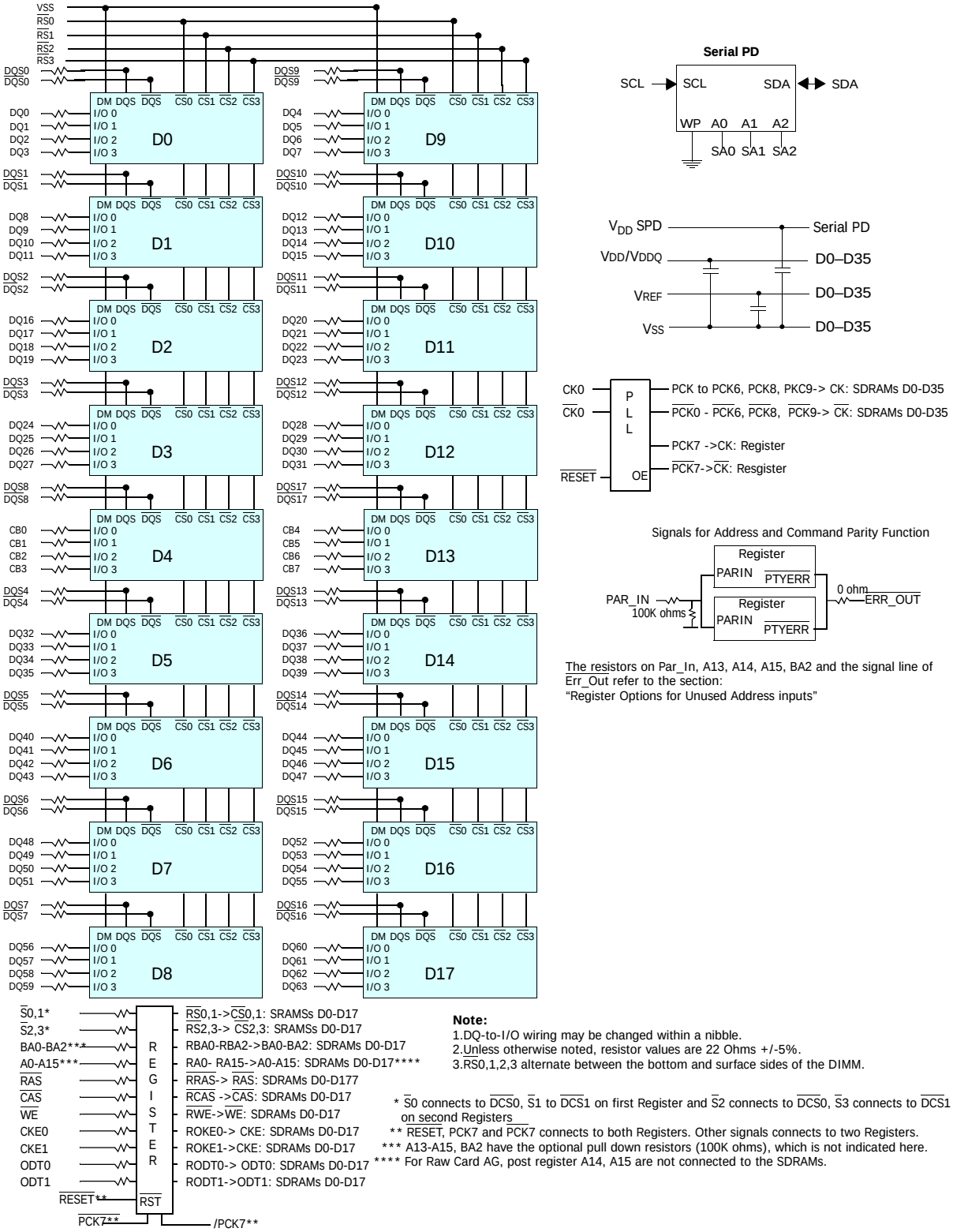
Register 1 share a part of Addr/Cmd input signal set.
Register 2 share the other part of Addr/Cmd input signal set.
0 Ohm resistor on Err_Out is not populated for non-parity card.

Notes:
1. DQ-to-I/O wiring may be changed within a nibble.
2. Unless otherwise noted, resistor values are 22 ohms +/-5%.
3. RS0 and RS1 alternate between the bottom and surface sides of the DIMM.

* S0 connects to DCS and S1 connects to CSR on Register1. S1 connects to DCS and S0 connects to CSR on Register 2.
** RESET, PCK7 and PCK7 connect to both Registers. Other signals connect to one of two Registers.
*** A13-15, BA2 have the optional pull down resistors(100K ohms), which is not indicated here.
**** For Raw Card AJ, post register A14, A15 are not connected to the SDRAMs.

FUNCTIONAL BLOCK DIAGRAM

8GB(256Mbx72) : HYMP41GP72CNP4L



Signals for Address and Command Parity Function

The resistors on Par_In, A13, A14, A15, BA2 and the signal line of Err_Out refer to the section:
"Register Options for Unused Address inputs"

Note:
1.DQ-to-I/O wiring may be changed within a nibble.
2.Unless otherwise noted, resistor values are 22 Ohms +/-5%.
3.RS0,1,2,3 alternate between the bottom and surface sides of the DIMM.

* S0 connects to DCS0, S1 to DCS1 on first Register and S2 connects to DCS0, S3 connects to DCS1 on second Registers
** RESET, PCK7 and PCK7 connects to both Registers. Other signals connects to two Registers.
*** A13-A15, BA2 have the optional pull down resistors (100K ohms), which is not indicated here.
**** For Raw Card AG, post register A14, A15 are not connected to the SDRAMs.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit	Note
Voltage on V_{DD} pin relative to Vss	V_{DD}	- 1.0 V ~ 2.3 V	V	1
Voltage on VDDL pin relative to Vss	V_{DDL}	-0.5V ~ 2.3 V	V	1
Voltage on V_{DDQ} pin relative to Vss	V_{DDQ}	- 0.5 V ~ 2.3 V	V	1
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	- 0.5 V ~ 2.3 V	V	1
Storage Temperature	T_{STG}	-50 ~ +100	^{o}C	1
Storage Humidity(without condensation)	H_{STG}	5 to 95	%	1

Note :

1. Stress greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Expousure to absolute maximum rating con ditions for extended periods may affect reliablility.

OPERATING CONDITIONS

Parameter	Symbol	Rating	Units	Notes
DIMM Operating temperature(ambient)	T_{OPR}	0 ~ +55	^{o}C	
DIMM Barometric Pressure(operating & storage)	P^{BAR}	105 to 69	K Pascal	1
DRAM Component Case Temperature Range	T_{CASE}	0 ~+95	^{o}C	2

Note :

1. Up to 9850 ft.
2. If the DRAM case temperature is Above 85^{o}C, the Auto-Refresh command interval has to be reduced to tREFI=3.9us. For Measurement conditions of T_{CASE}, please refer to the JEDEC document JESD51-2.

DC OPERATING CONDITIONS (SSTL_1.8)

Parameter	Symbol	Min	Max	Unit	Note
Power Supply Voltage	V_{DD}	1.7	1.9	V	
	V_{DDL}	1.7	1.9	V	
	V_{DDQ}	1.7	1.9	V	1
Input Reference Voltage	V_{REF}	0.49 x V_{DDQ}	0.51 x V_{DDQ}	V	2
EEPROM Supply Voltage	V_{DDSPD}	1.7	3.6	V	
Termination Voltage	V_{TT}	V_{REF}-0.04	V_{REF}+0.04	V	3

Note :

1. V_{DDQ} must be less than or equal to V_{DD}.
2. Peak to peak ac noise on V_{REF} may not exeed +/-2% V_{REF}(dc)
3. VTT of transmitting device must track VREF of receiving device.

INPUT DC LOGIC LEVEL

Parameter	Symbol	Min	Max	Unit	Notes
Input High Voltage	V_{IH}(DC)	V_{REF} + 0.125	V_{DDQ} + 0.3	V	
Input Low Voltage	V_{IL}(DC)	-0.30	V_{REF} - 0.125	V	

INPUT AC LOGIC LEVEL

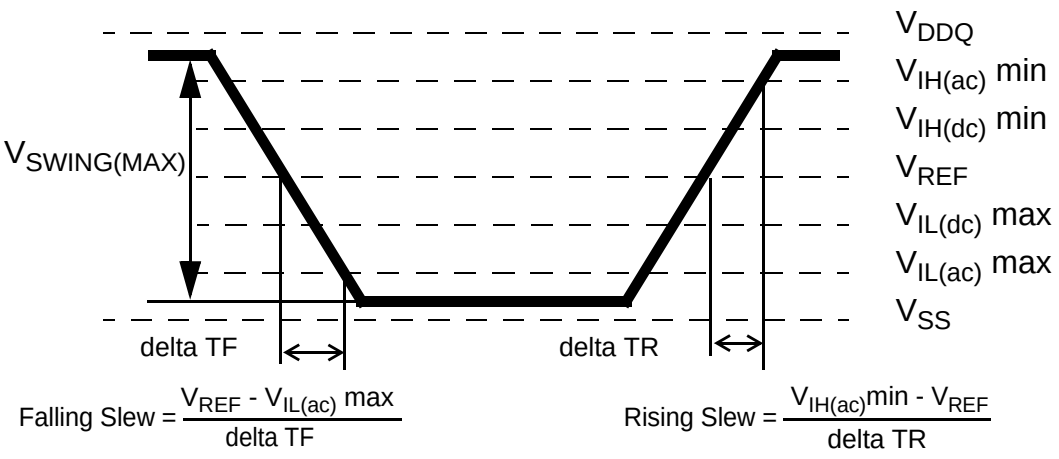
Parameter	Symbol	DDR2 400/533		DDR2 667/800		Unit	Notes
		Min	Max	Min	Max		
AC Input logic High	V_{IH}(AC)	V_{REF} + 0.250	-	V_{REF} + 0.200	-	V	
AC Input logic Low	V_{IL}(AC)	-	V_{REF} - 0.250	-	V_{REF} - 0.200	V	

AC INPUT TEST CONDITIONS

Symbol	Condition	Value	Units	Notes
V_{REF}	Input reference voltage	0.5 * V_{DDQ}	V	1
$V_{SWING(MAX)}$	Input signal maximum peak to peak swing	1.0	V	1
SLEW	Input signal minimum slew rate	1.0	V/ns	2, 3

Notes:

1. Input waveform timing is referenced to the input signal crossing through the V_{REF} level applied to the device under test.
2. The input signal minimum slew rate is to be maintained over the range from V_{REF} to $V_{IH(ac)\ min}$ for rising edges and the range from V_{REF} to $V_{IL(ac)\ max}$ for falling edges as shown in the below figure.
3. AC timings are referenced with input waveforms switching from VIL(ac) to VIH(ac) on the positive transitions and VIH(ac) to VIL(ac) on the negative transitions.

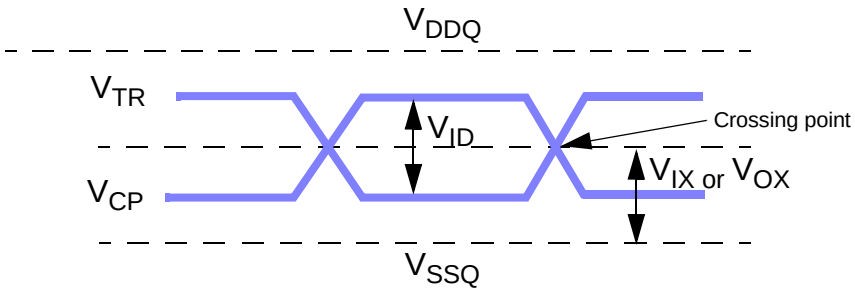


< Figure : AC Input Test Signal Waveform>

Differential Input AC logic Level

Symbol	Parameter	Min.	Max.	Units	Note
V_{ID} (ac)	ac differential input voltage	0.5	V_{DDQ} + 0.6	V	1
V_{IX} (ac)	ac differential cross point voltage	0.5 * V_{DDQ} - 0.175	0.5 * V_{DDQ} + 0.175	V	2

1. V_{IN}(DC) specifies the allowable DC execution of each input of differential pair such as CK, $\overline{CK}$, DQS, $\overline{DQS}$, LDQS, $\overline{LDQS}$, UDQS and $\overline{UDQS}$.
2. V_{ID}(DC) specifies the input differential voltage $|V_{TR} - V_{CP}|$ required for switching, where V_{TR} is the true input (such as CK, DQS, LDQS or UDQS) level and V_{CP} is the complementary input (such as $\overline{CK}$, $\overline{DQS}$, $\overline{LDQS}$ or $\overline{UDQS}$) level. The minimum value is equal to V_{IH}(DC) - V_{IL}(DC).



< Differential signal levels >

Notes:

1. V_{ID}(AC) specifies the input differential voltage $|V_{TR} - V_{CP}|$ required for switching, where V_{TR} is the true input signal (such as CK, DQS, LDQS or UDQS) and V_{CP} is the complementary input signal (such as $\overline{CK}$, $\overline{DQS}$, $\overline{LDQS}$ or $\overline{UDQS}$). The minimum value is equal to V_{IH}(AC) - V_{IL}(AC).
2. The typical value of V_{IX}(AC) is expected to be about 0.5 * V_{DDQ} of the transmitting device and V_{IX}(AC) is expected to track variations in V_{DDQ} . V_{IX}(AC) indicates the voltage at whitch differential input signals must cross.

DIFFERENTIAL AC OUTPUT PARAMETERS

Symbol	Parameter	Min.	Max.	Units	Note
V_{OX} (ac)	ac differential cross point voltage	0.5 * V_{DDQ} - 0.125	0.5 * V_{DDQ} + 0.125	V	1

Note:

1. The typical value of V_{OX}(AC) is expected to be about 0.5 * V_{DDQ} of the transmitting device and V_{OX}(AC) is expected to track variations in V_{DDQ} . V_{OX}(AC) indicates the voltage at whitch differential output signals must cross.

OUTPUT BUFFER LEVELS

OUTPUT AC TEST CONDITIONS

Symbol	Parameter	SSTL_18	Units	Notes
V_{OTR}	Output Timing Measurement Reference Level	0.5 * V_{DDQ}	V	1

Notes:

1. The VDDQ of the device under test is referenced.

OUTPUT DC CURRENT DRIVE

Symbol	Parameter	SSTl_18	Units	Notes
$I_{OH(dc)}$	Output Minimum Source DC Current	- 13.4	mA	1, 3, 4
$I_{OL(dc)}$	Output Minimum Sink DC Current	13.4	mA	2, 3, 4

Notes:

1. V_{DDQ} = 1.7 V; V_{OUT} = 1420 mV. (V_{OUT} - V_{DDQ})/I_{OH} must be less than 21 ohm for values of V_{OUT} between V_{DDQ} and V_{DDQ} - 280 mV.
2. V_{DDQ} = 1.7 V; V_{OUT} = 280 mV. V_{OUT}/I_{OL} must be less than 21 ohm for values of V_{OUT} between 0 V and 280 mV.
3. The dc value of V_{REF} applied to the receiving device is set to V_{TT}
4. The values of I_{OH}(dc) and I_{OL}(dc) are based on the conditions given in Notes 1 and 2. They are used to test device drive current capability to ensure V_{IH} min plus a noise margin and V_{IL} max minus a noise margin are delivered to an SSTL_18 receiver.
   The actual current values are derived by shifting the desired driver operating point along a 21 ohm load line to define a convenient driver current for measurement.

PIN Capacitance (VDD=1.8V,VDDQ=1.8V, TA=25℃. f=1MHz)

1GB : HYMP112P72CP8L

Pin	Symbol	Min	Max	Unit
CK0, $\overline{CK0}$	CCK	7	11	pF
CKE, ODT	CI1	8	12	pF
$\overline{CS}$	CI2	8	12	pF
Address, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	CI3	8	12	pF
DQ, DM, DQS, $\overline{DQS}$	CIO	6	9	pF

2GB : HYMP125P72CP4L

Pin	Symbol	Min	Max	Unit
CK0, $\overline{CK0}$	CCK	7	11	pF
CKE, ODT	CI1	8	12	pF
$\overline{CS}$	CI2	10	15	pF
Address, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	CI3	8	12	pF
DQ, DM, DQS, $\overline{DQS}$	CIO	6	9	pF

4GB : HYMP351P72CMP4L

Pin	Symbol	Min	Max	Unit
CK0, $\overline{CK0}$	CCK	9.5	10.4	pF
CKE, ODT	CI1	10.5	16	pF
$\overline{CS}$	CI2	10.5	16	pF
Address, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	CI3	10.5	16	pF
DQ, DM, DQS, $\overline{DQS}$	CIO	17	21	pF

8GB : HYMP41GP72CNP4L

Pin	Symbol	Min	Max	Unit
CK0, $\overline{CK0}$	CCK	7	11	pF
CKE, ODT	CI1	8	12	pF
$\overline{CS}$	CI2	8	12	pF
Address, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	CI3	10	15	pF
DQ, DM, DQS, $\overline{DQS}$	CIO	18	22	pF

Note :

1. Pins not under test are tied to GND.
2. These value are guaranteed by design and tested on a sample basis only.

IDD SPECIFICATIONS (T_{CASE} : 0 to 95°C)

1GB, 128M x 72 VLP Registered DIMM : HYMP112P72CP8L

Symbol	C4 (533@CL4)	Y5 (667@CL5)	S6 (800@CL6)	Unit	Notes
IDD0	1235	1280	1325	mA	
IDD1	1325	1370	1415	mA	
IDD2P	740	740	740	mA	
IDD2Q	893	920	938	mA	
IDD2N	965	1010	1055	mA	
IDD3P-F	830	875	875	mA	
IDD3P-S	758	758	758	mA	
IDD3N	1055	1100	1145	mA	
IDD4W	1775	2000	2180	mA	
IDD4R	1775	2000	2180	mA	
IDD5	2135	2225	2225	mA	1
IDD6	540	540	540	mA	
IDD7	2225	2270	2315	mA	

2GB, 256M x 72 VLP Registered DIMM : HYMP125P72CP4L

Symbol	C4 (533@CL4)	Y5 (667@CL5)	S6 (800@CL6)	Unit	Notes
IDD0	1820	1910	2000	mA	
IDD1	2000	2090	2180	mA	
IDD2P	830	830	830	mA	
IDD2Q	1136	1190	1226	mA	
IDD2N	1280	1370	1460	mA	
IDD3P-F	1010	1100	1100	mA	
IDD3P-S	866	866	866	mA	
IDD3N	1460	1550	1640	mA	
IDD4W	2900	3350	3710	mA	
IDD4R	2900	3350	3710	mA	
IDD5	3620	3800	3600	mA	1
IDD6	630	630	630	mA	
IDD7	3800	3890	3980	mA	

Notes :

1. IDD6 current values are guaranteed up to Tcase of 85°C max.

4GB, 256M x 72 VLP Registered DIMM : HYMP351P72CMP4L

Symbol	C4 (533@CL4)	Y5 (667@CL5)	S6 (800@CL6)	Unit	Notes
IDD0	2630	2810	2990	mA	
IDD1	2810	2990	3170	mA	
IDD2P	1010	1010	1010	mA	
IDD2Q	1622	1730	1802	mA	
IDD2N	1910	2090	2270	mA	
IDD3P-F	1370	1550	1550	mA	
IDD3P-S	1082	1082	1082	mA	
IDD3N	2270	2450	2630	mA	
IDD4W	3710	4250	4700	mA	
IDD4R	3710	4250	4700	mA	
IDD5	4430	4700	4790	mA	1
IDD6	810	810	810	mA	
IDD7	4610	4790	4970	mA	

8GB, 256M x 72 VLP Registered DIMM : HYMP41GP72CNP4L

Symbol	C4 (533@CL4)	Y5 (667@CL5)	Unit	Notes
IDD0	TBD	TBD	mA	
IDD1	TBD	TBD	mA	
IDD2P	TBD	TBD	mA	
IDD2Q	TBD	TBD	mA	
IDD2N	TBD	TBD	mA	
IDD3P-F	TBD	TBD	mA	
IDD3P-S	TBD	TBD	mA	
IDD3N	TBD	TBD	mA	
IDD4W	TBD	TBD	mA	
IDD4R	TBD	TBD	mA	
IDD5	TBD	TBD	mA	1
IDD6	TBD	TBD	mA	
IDD7	TBD	TBD	mA	

IDD Measurement Conditions

Symbol	Conditions		Units
IDD0	**Operating one bank active-precharge current**; t_{CK} = $t_{CK(IDD)}$, t_{RC} = $t_{RC(IDD)}$, t_{RAS} = $t_{RAS-min(IDD)}$;CKE is HIGH, $\overline{CS}$ is HIGH between valid commands;Address bus inputs are SWITCHING;Data bus inputs are SWITCHING		mA
IDD1	**Operating one bank active-read-precharge curren** ; IOUT = 0mA;BL = 4, CL = CL(IDD), AL = 0; t_{CK} = $t_{CK(IDD)}$, t_{RC} = t_{RC} (IDD), t_{RAS} = $t_{RASmin(IDD)}$, t_{RCD} = $t_{RCD(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands ; Address bus inputs are SWITCHING ; Data pattern is same as IDD4W		mA
IDD2P	**Precharge power-down current** ; All banks idle ; t_{CK} = $t_{CK(IDD)}$; CKE is LOW ; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		mA
IDD2Q	**Precharge quiet standby current**;All banks idle; t_{CK} = $t_{CK(IDD)}$;CKE is HIGH, $\overline{CS}$ is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		mA
IDD2N	**Precharge standby current**; All banks idle; t_{CK} = $t_{CK(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA
IDD3P	**Active power-down current**; All banks open; t_{CK} = $t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0	mA
		Slow PDN Exit MRS(12) = 1	mA
IDD3N	**Active standby current**; All banks open; t_{CK} = $t_{CK(IDD)}$, t_{RAS} = $t_{RASmax(IDD)}$, t_{RP} =$t_{RP(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA
IDD4W	**Operating burst write current**; All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; t_{CK} = $t_{CK(IDD)}$, t_{RAS} = $t_{RASmax(IDD)}$, t_{RP} = $t_{RP(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA
IDD4R	**Operating burst read current**; All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; t_{CK} = $t_{CK(IDD)}$, t_{RAS} = $t_{RASmax(IDD)}$, t_{RP} = $t_{RP(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING;; Data pattern is same as IDD4W		mA
IDD5B	**Burst refresh current**; t_{CK} = $t_{CK(IDD)}$; Refresh command at every $t_{RFC(IDD)}$ interval; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA
IDD6	**Self refresh current**; CK and $\overline{CK}$ at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING. IDD6 current values are guaranted up to Tcase of 85℃ max.		mA
IDD7	**Operating bank interleave read current**; All bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = t_{RCD}(IDD)-1*t_{CK}(IDD); t_{CK} = $t_{CK(IDD)}$, t_{RC} = $t_{RC(IDD)}$, t_{RRD} = $t_{RRD(IDD)}$, t_{RCD} = 1*$t_{CK(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R; - Refer to the following page for detailed timing conditions		mA

Notes:

1. IDD specifications are tested after the device is properly initialized
2. Input slew rate is specified by AC Parametric Test Condition
3. IDD parameters are specified with ODT disabled.
4. Data bus consists of DQ, DM, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$, LDQS, $\overline{LDQS}$, UDQS, and $\overline{UDQS}$. IDD values must be met with all combinations of EMRS bits 10 and 11.
5. Definitions for IDD
   LOW is defined as Vin ≤ VILAC(max)
   HIGH is defined as Vin ≥ VIHAC(min)
   STABLE is defined as inputs stable at a HIGH or LOW level
   FLOATING is defined as inputs at VREF = VDDQ/2
   SWITCHING is defined as: inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and control signals, and inputs changing between HIGH and LOW every other data transfer (once per clock) for DQ signals not including masks or strobes.

Electrical Characteristics & AC Timings

Speed Bins and CL,tRCD,tRP,tRC and tRAS for Corresponding Bin

Speed	DDR2-800(S6)	DDR2-667(Y5)	DDR2-533 (C4)	DDR2-400 (E3)	Unit
Bin(CL-tRCD-tRP)	6-6-6	5-5-5	4-4-4	3-3-3	
Parameter	min	min	min	min	
CAS Latency	6	5	4	3	ns
tRCD	15	15	15	15	ns
tRP	15	15	15	15	ns
tRC	60	60	60	55	ns
tRAS	45	45	45	40	ns

AC Timing Parameters by Speed Grade

Parameter	Symbol	DDR2-400		DDR2-533		Unit	Note
		Min	Max	Min	Max		
Data-Out edge to Clock edge Skew	tAC	-600	600	-500	500	ps	
DQS-Out edge to Clock edge Skew	tDQSCK	-500	500	-500	450	ns	
Clock High Level Width	tCH	0.45	0.55	0.45	0.55	CK	
Clock Low Level Width	tCL	0.45	0.55	0.45	0.55	CK	
Clock Half Period	tHP	min (tCL,tCH)	-	min (tCL,tCH)	-	ns	
System Clock Cycle Time	tCK	5000	8000	3750	8000	ps	
DQ and DM input setup time	tDS	150	-	100	-	ps	1
DQ and DM input hold time	tDH	275	-	225	-	ps	1
Control & Address input Pulse Width for each input	tIPW	0.6	-	0.6	-	tCK	
DQ and DM input pulse witdth for each input pulse width for each input	tDIPW	0.35	-	0.35	-	tCK	
Data-out high-impedance window from CK, /CK	tHZ	-	tAC max	-	tAC max	ps	
DQS low-impedance time from CK/$\overline{CK}$	tLZ(DQS)	tAC min	tAC max	tAC min	tAC max	ps	
DQ low-impedance time from CK/$\overline{CK}$	tLZ(DQ)	2*tAC min	tAC max	2*tAC min	tAC max	ps	
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	-	350	-	300	ps	
DQ hold skew factor	tQHS	-	450	-	400	ps	
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	-	tHP - tQHS	-	ps	
Write command to first DQS latching transition	tDQSS	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	tCK	
DQS input high pulse width	tDQSH	0.35	-	0.35	-	tCK	
DQS input low pulse width	tDQSL	0.35	-	0.35	-	tCK	
DQS falling edge to CK setup time	tDSS	0.2	-	0.2	-	tCK	
DQS falling edge hold time from CK	tDSH	0.2	-	0.2	-	tCK	
Mode register set command cycle time	tMRD	2	-	2	-	tCK	
Write preamble	tWPRE	0.35	-	0.35	-	tCK	
Write postamble	tWPST	0.4	0.6	0.4	0.6	tCK	

- continued -

Parameter	Symbol	DDR2-400		DDR2-533		Unit	Note
		Min	Max	Min	Max		
Address and control input setup time	tIS	350	-	250	-	ps	
Address and control input hold time	tIH	475	-	375	-	ps	
Read preamble	tRPRE	0.9	1.1	0.9	1.1	tCK	
Read postamble	tRPST	0.4	0.6	0.4	0.6	tCK	
Auto-Refresh to Active/Auto-Refresh command period	tRFC	127.5	-	127.5	-	ns	
Row Active to Row Active Delay for 1KB page size	tRRD	7.5	-	7.5	-	ns	
Row Active to Row Active Delay for 2KB page size	tRRD	10	-	10	-	ns	
Four Activate Window for 1KB page size	tFAW	37.5	-	37.5	-	ns	
Four Activate Window for 2KB page size	tFAW	50	-	50	-	ns	
$\overline{CAS}$ to $\overline{CAS}$ command delay	tCCD	2		2		tCK	
Write recovery time	tWR	15	-	15	-	ns	
Auto Precharge Write Recovery + Precharge Time	tDAL	tWR+tRP	-	tWR+tRP	-	tCK	
Write to Read Command Delay	tWTR	10	-	7.5	-	ns	
Internal read to precharge command delay	tRTP	7.5		7.5		ns	
Exit self refresh to a non-read command	tXSNR	tRFC + 10		tRFC + 10		ns	
Exit self refresh to a read command	tXSRD	200	-	200	-	tCK	
Exit precharge power down to any non-read command	tXP	2	-	2	-	tCK	
Exit active power down to read command	tXARD	2		2		tCK	
Exit active power down to read command (Slow exit, Lower power)	tXARDS	6 - AL		6 - AL		tCK	
CKE minimum pulse width (high and low pulse width)	tCKE	3		3		tCK	
ODT turn-on delay	tAOND	2	2	2	2	tCK	
ODT turn-on	tAON	tAC(min)	tAC(max)+1	tAC(min)	tAC(max)+1	ns	
ODT turn-on(Power-Down mode)	tAONPD	tAC(min)+2	2tCK+tAC(max)+1	tAC(min)+2	2tCK+tAC(max)+1	ns	
ODT turn-off delay	tAOFD	2.5	2.5	2.5	2.5	tCK	
ODT turn-off	tAOF	tAC(min)	tAC(max)+0.6	tAC(min)	tAC(max)+0.6	ns	
ODT turn-off (Power-Down mode)	tAOFPD	tAC(min)+2	2.5tCK+tAC(max)+1	tAC(min)+2	2.5tCK+tAC(max)+1	ns	
ODT to power down entry latency	tANPD	3		3		tCK	
ODT power down exit latency	tAXPD	8		8		tCK	
OCD drive mode output delay	tOIT	0	12	0	12	ns	
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS+tCK+tIH		tIS+tCK+tIH		ns	
Average periodic Refresh Interval	tREFI	-	7.8	-	7.8	us	2
	tREFI	-	3.9	-	3.9	us	3

Note :

1. For details and notes, please refer to the relevant HYNIX component datasheet (HY5PS1G[4,8]31CFP).
2. 0°C ≤ TCASE ≤ 85°C
3. 85°C < TCASE ≤ 95°C

Parameter	Symbol	DDR2-667		DDR2-800		Unit	Note
		min	max	min	max		
DQ output access time from CK/$\overline{CK}$	tAC	-450	+450	-400	+400	ps	
DQS output access time from CK/$\overline{CK}$	tDQSCK	-400	+400	-350	+350	ps	
CK high-level width	tCH	0.45	0.55	0.45	0.55	tCK	
CK low-level width	tCL	0.45	0.55	0.45	0.55	tCK	
CK half period	tHP	min(tCL, tCH)	-	min(tCL, tCH)	-	ps	
Clock cycle time, CL=x	tCK	3000	8000	2500		ps	
DQ and DM input setup time (differential strobe)	tDS	100	-	50	-	ps	1
DQ and DM input hold time (differential strobe)	tDH	175	-	125	-	ps	1
Control & Address input pulse width for each input	tIPW	0.6	-	0.6	-	tCK	
DQ and DM input pulse width for each input	tDIPW	0.35	-	0.35	-	tCK	
Data-out high-impedance time from CK/$\overline{CK}$	tHZ	-	tAC max	-	tAC max	ps	
DQS low-impedance time from CK/$\overline{CK}$	tLZ(DQS)	tAC min	tAC max	tAC min	tAC max	ps	
DQ low-impedance time from CK/$\overline{CK}$	tLZ(DQ)	2*tAC min	tAC max	2*tAC min	tAC max	ps	
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	-	240	-	200	ps	
DQ hold skew factor	tQHS	-	340	-	300	ps	
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	-	tHP - tQHS	-	ps	
First DQS latching transition to associated clock edge	tDQSS	- 0.25	+ 0.25	- 0.25	+ 0.25	tCK	
DQS input high pulse width	tDQSH	0.35	-	0.35	-	tCK	
DQS input low pulse width	tDQSL	0.35	-	0.35	-	tCK	
DQS falling edge to CK setup time	tDSS	0.2	-	0.2	-	tCK	
DQS falling edge hold time from CK	tDSH	0.2	-	0.2	-	tCK	
Mode register set command cycle time	tMRD	2	-	2	-	tCK	
Write preamble	tWPRE	0.35	-	0.35	-	tCK	
Write postamble	tWPST	0.4	0.6	0.4	0.6	tCK	
Address and control input setup time	tIS	200	-	175	-	ps	
Address and control input hold time	tIH	275	-	250	-	ps	
Read preamble	tRPRE	0.9	1.1	0.9	1.1	tCK	
Read postamble	tRPST	0.4	0.6	0.4	0.6	tCK	
Auto-Refresh to Active/Auto-Refresh command period	tRFC	127.5	-	127.5	-	ns	
Active to active command period for 1KB page size products	tRRD	7.5	-	7.5	-	ns	
Active to active command period for 2KB page size products	tRRD	10	-	10	-	ns	
Four Active Window for 1KB page size products	tFAW	37.5	-	35	-	ns	
Four Active Window for 2KB page size products	tFAW	50	-	45	-	ns	

- continued -

Parameter	Symbol	DDR2-667		DDR2-800		Unit	Note
		min	max	min	max		
$\overline{CAS}$ to $\overline{CAS}$ command delay	tCCD	2		2		tCK	
Write recovery time	tWR	15	-	15	-	ns	
Auto precharge write recovery + precharge time	tDAL	WR+tRP	-	WR+tRP	-	tCK	
Internal write to read command delay	tWTR	7.5	-	7.5	-	ns	
Internal read to precharge command delay	tRTP	7.5		7.5		ns	
Exit self refresh to a non-read command	tXSNR	tRFC + 10		tRFC + 10		ns	
Exit self refresh to a read command	tXSRD	200	-	200	-	tCK	
Exit precharge power down to any non-read command	tXP	2	-	2	-	tCK	
Exit active power down to read command	tXARD	2		2		tCK	
Exit active power down to read command (Slow exit, Lower power)	tXARDS	7 - AL		8 - AL		tCK	
CKE minimum pulse width (high and low pulse width)	tCKE	3		3		tCK	
ODT turn-on delay	tAOND	2	2	2	2	tCK	
ODT turn-on	tAON	tAC(min)	tAC(max) +0.7	tAC(min)	tAC(max) +0.7	ns	
ODT turn-on(Power-Down mode)	tAONPD	tAC(min)+2	2tCK+ tAC(max)+1	tAC(min) +2	2tCK+ tAC(max)+1	ns	
ODT turn-off delay	tAOFD	2.5	2.5	2.5	2.5	tCK	
ODT turn-off	tAOF	tAC(min)	tAC(max)+ 0.6	tAC(min)	tAC(max) +0.6	ns	
ODT turn-off (Power-Down mode)	tAOFPD	tAC(min) +2	2.5tCK+ tAC(max)+1	tAC(min) +2	2.5tCK+ tAC(max)+1	ns	
ODT to power down entry latency	tANPD	3		3		tCK	
ODT power down exit latency	tAXPD	8		8		tCK	
OCD drive mode output delay	tOIT	0	12	0	12	ns	
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS+tCK+tIH		tIS+tCK +tIH		ns	
Average periodic Refresh Interval	tREFI	-	7.8	-	7.8	us	2
	tREFI	-	3.9	-	3.9	us	3

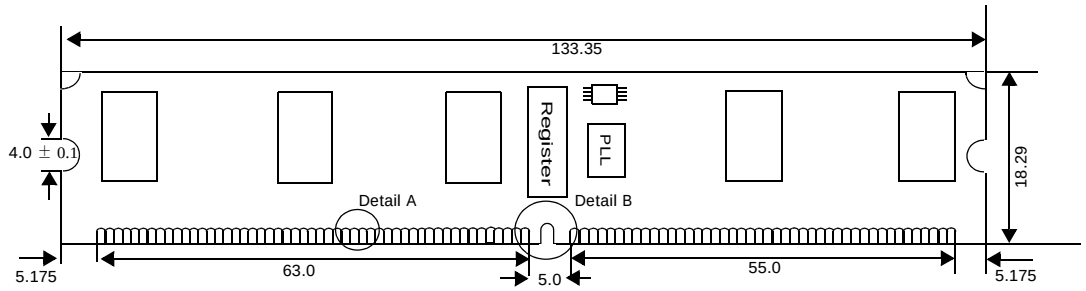
Note :

1. For details and notes, please refer to the relevant HYNIX component datasheet (HY5PS1G[4,8]31CFP).
2. 0°C ≤ TCASE ≤ 85°C
3. 85°C < TCASE ≤ 95°C

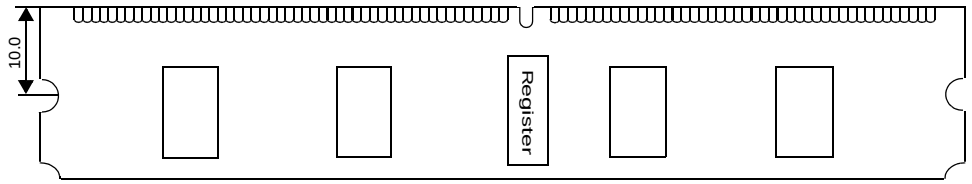
PACKAGE OUTLINE

128Mx72 (1 rank) - HYMP112P72CP8L

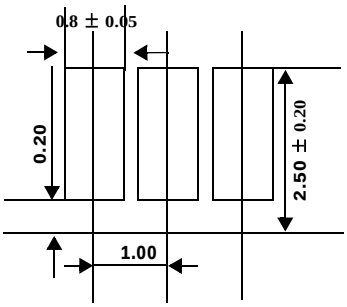
Front



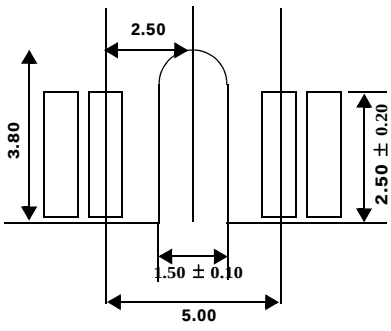
Back



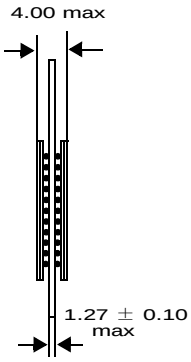
Detail of Contacts A



Detail of Contacts B



Side

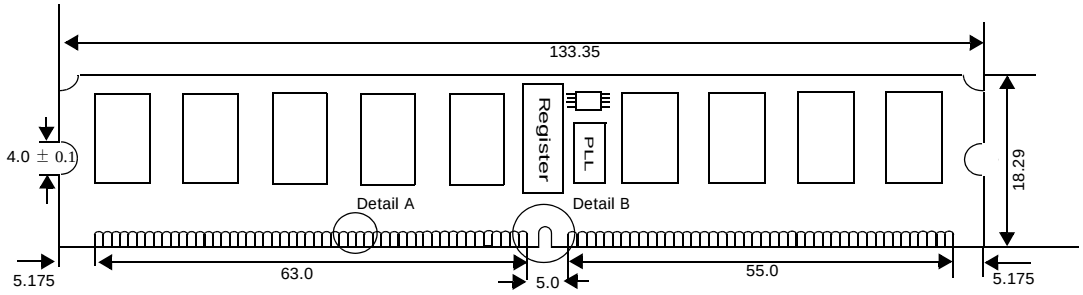


Note) All dimensions are in millimeters unless otherwise stated.

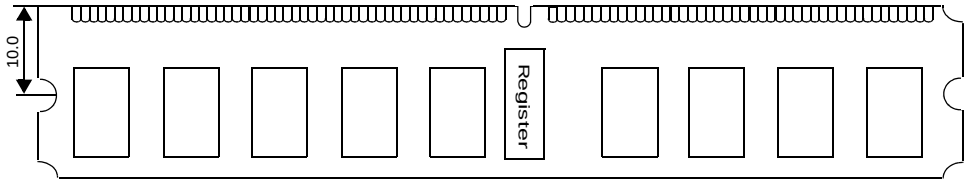
PACKAGE OUTLINE

256Mx72 (1 rank) - HYMP125P72CP4L

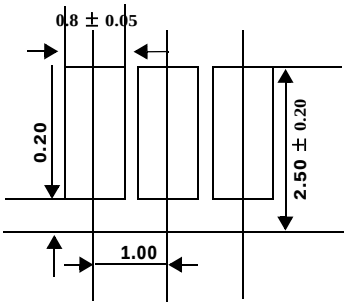
Front



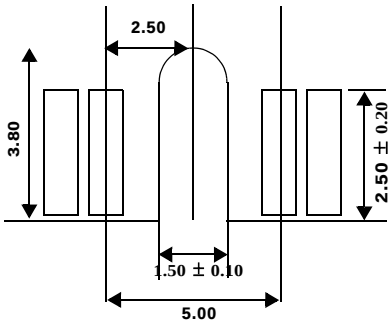
Back



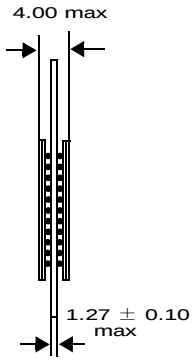
Detail of Contacts A



Detail of Contacts B



Side

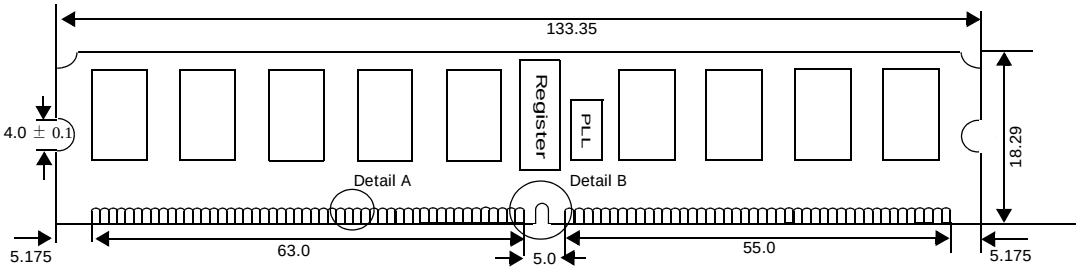


Note) All dimensions are in millimeters unless otherwise stated.

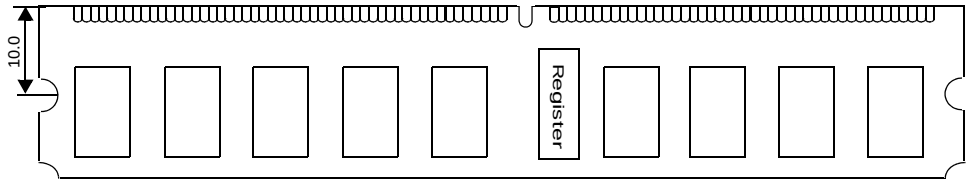
PACKAGE OUTLINE

256Mx72 (2 rank) - HYMP351P72CMP4L

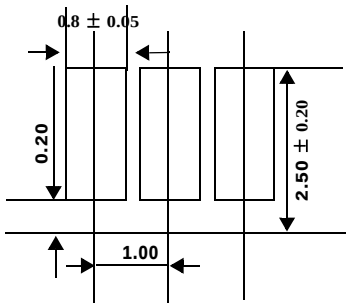
Front



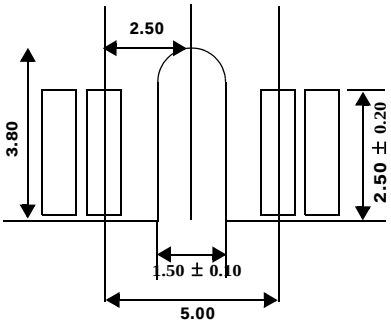
Back



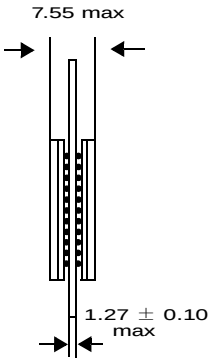
Detail of Contacts A



Detail of Contacts B



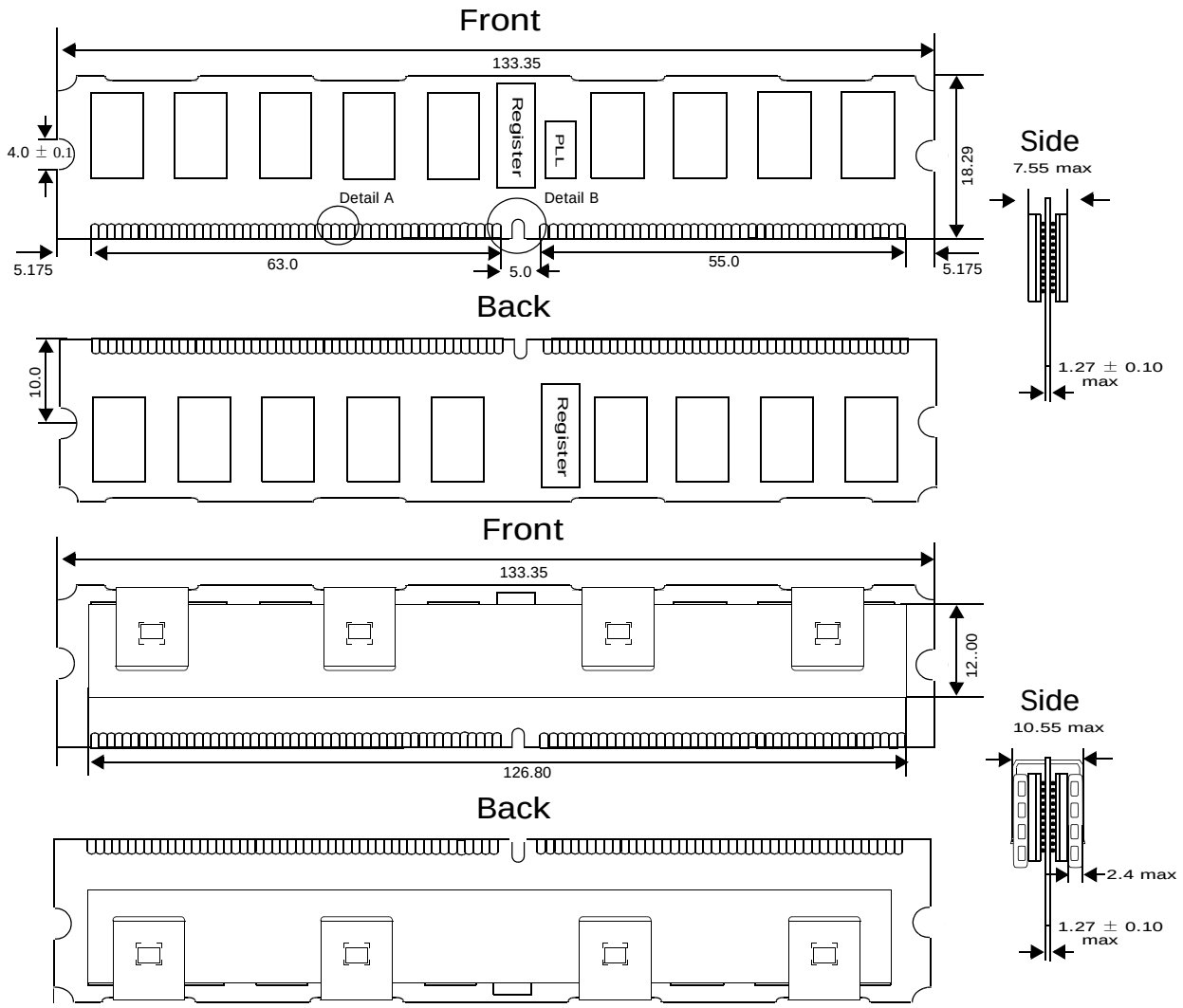
Side

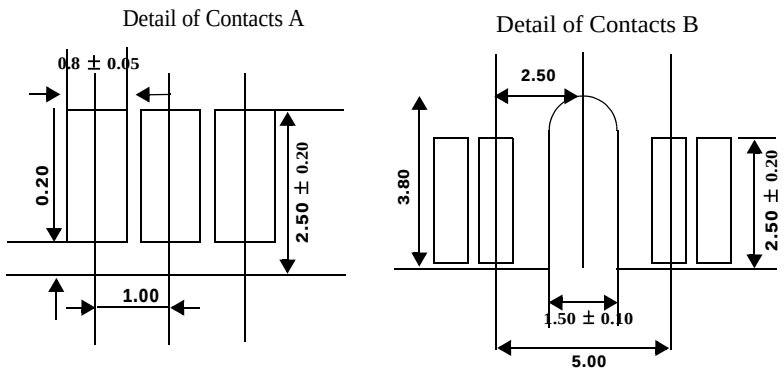


Note) All dimensions are in millimeters unless otherwise stated.

PACKAGE OUTLINE

256Mx72 (4 rank) - HYMP41GP72CNP4L





Note) All dimensions are in millimeters unless otherwise stated.

REVISION HISTORY

Revision	History	Date	Remark
0.1	Initial Release	Aug. 2007	
0.2	8GB added, IDD updated	May. 2008	