

## P-channel 60 V, 0.025 $\Omega$ typ., 35 A STripFET™ F6 Power MOSFET in a DPAK package

Datasheet - production data

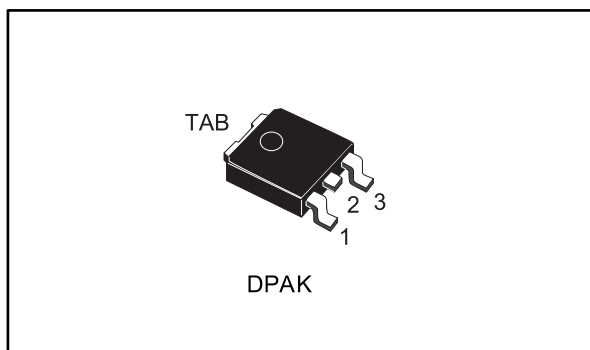
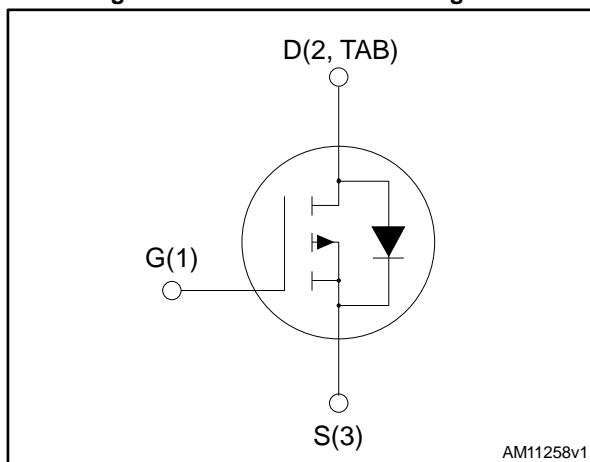


Figure 1: Internal schematic diagram



### Features

Order code	V <sub>DSS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>	P <sub>TOT</sub>
STD35P6LLF6	60 V	0.028 $\Omega$	35 A	70 W

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

### Applications

- Switching applications

### Description

This device is a P-channel Power MOSFET developed using the STripFET™ F6 technology, with a new trench gate structure. The resulting Power MOSFET exhibits very low R<sub>DS(on)</sub> in all packages.

Table 1: Device summary

Order code	Marking	Package	Packaging
STD35P6LLF6	35P6LLF6	DPAK	Tape and Reel

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# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	60	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	35	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	25	A
$I_{DM}^{(1)}$	Drain current (pulsed)	140	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	70	W
$T_{stg}$	Storage temperature range	-55 to 175	$^\circ\text{C}$
$T_j$	Operating junction temperature range		

**Notes:**

<sup>(1)</sup>Pulse width limited by safe operating area.

**Table 3: Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	2.14	$^\circ\text{C/W}$



For the P-channel Power MOSFET, current polarity of voltages and current have to be reversed.

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 4: Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$	60			V
$I_{DSS}$	Zero gate voltage Drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 60\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 60\text{ V}$ , $T_C = 125\text{ °C}^{(1)}$			10	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	1		2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 17.5\text{ A}$		0.025	0.028	$\Omega$
		$V_{GS} = 4.5\text{ V}$ , $I_D = 17.5\text{ A}$		0.03	0.036	

**Notes:**

<sup>(1)</sup>Defined by design, not subject to production test.

**Table 5: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	3780	-	pF
$C_{oss}$	Output capacitance		-	262	-	pF
$C_{rss}$	Reverse transfer capacitance		-	170	-	pF
$Q_g$	Total gate charge	$V_{DD} = 30\text{ V}$ , $I_D = 35\text{ A}$ , $V_{GS} = 0\text{ to }4.5\text{ V}$ (see <a href="#">Figure 14: "Gate charge test circuit"</a> )	-	30	-	nC
$Q_{gs}$	Gate-source charge		-	10.8	-	nC
$Q_{gd}$	Gate-drain charge		-	10.5	-	nC
$R_G$	Gate input resistance	$I_D = 0\text{ A}$ , gate DC bias = $0\text{ V}$ , $f = 1\text{ MHz}$ , magnitude of alternative signal = $20\text{ mV}$	-	1.7	-	$\Omega$

**Table 6: Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 30\text{ V}$ , $I_D = 17.5\text{ A}$ $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 13: "Switching times test circuit for resistive load"</a> )	-	51.4	-	ns
$t_r$	Rise time		-	39	-	ns
$t_{d(off)}$	Turn-off-delay time		-	171	-	ns
$t_f$	Fall time		-	21	-	ns



For the P-channel Power MOSFET, current polarity of voltages and current have to be reversed.

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$V_{GS} = 0 \text{ V}$ , $I_{SD} = 35 \text{ A}$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 35 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ , $V_{DD} = 48 \text{ V}$ , (see <a href="#">Figure 15</a> : "Test circuit for inductive load switching and diode recovery times")	-	34		ns
$Q_{rr}$	Reverse recovery charge		-	48		nC
$I_{RRM}$	Reverse recovery current		-	2.8		A

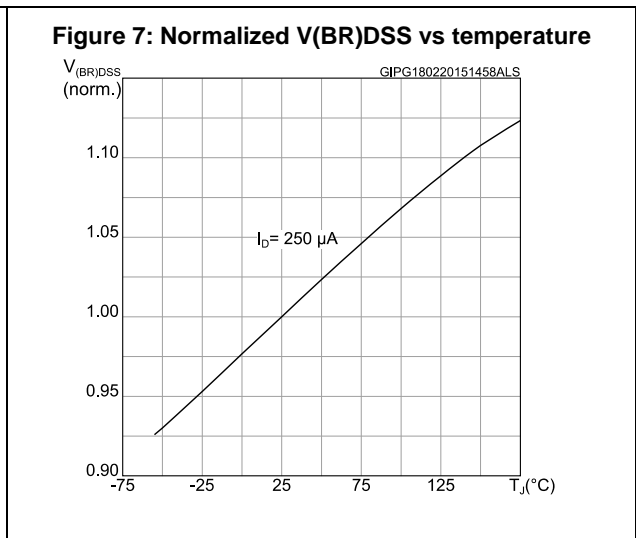
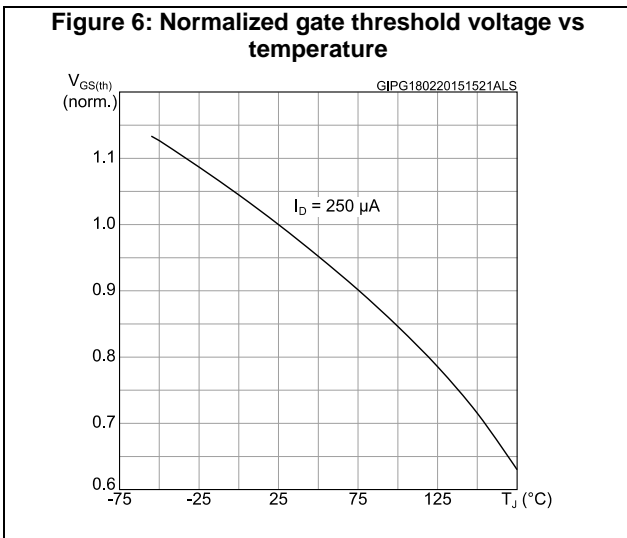
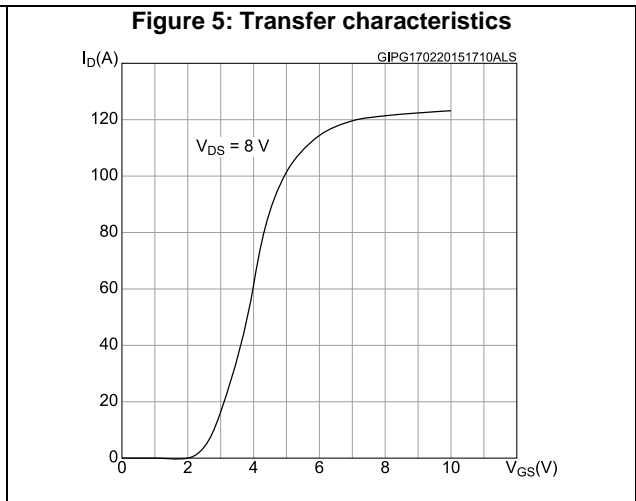
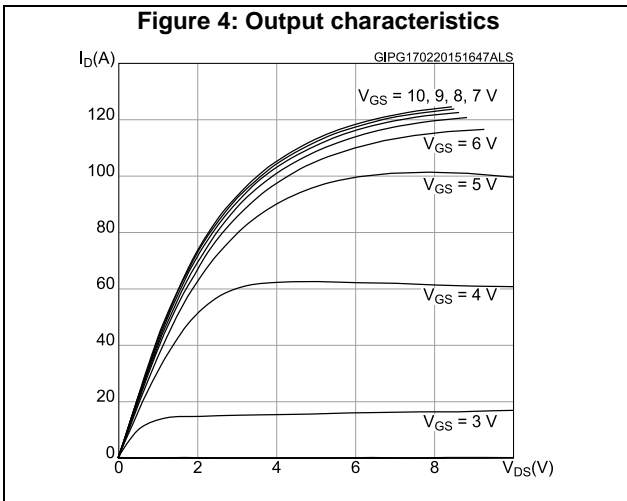
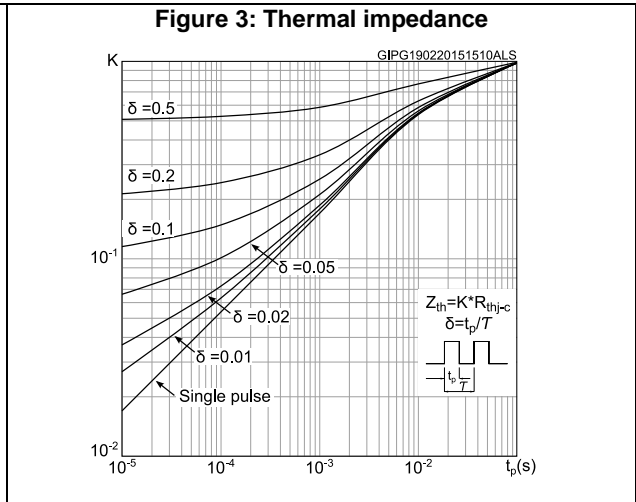
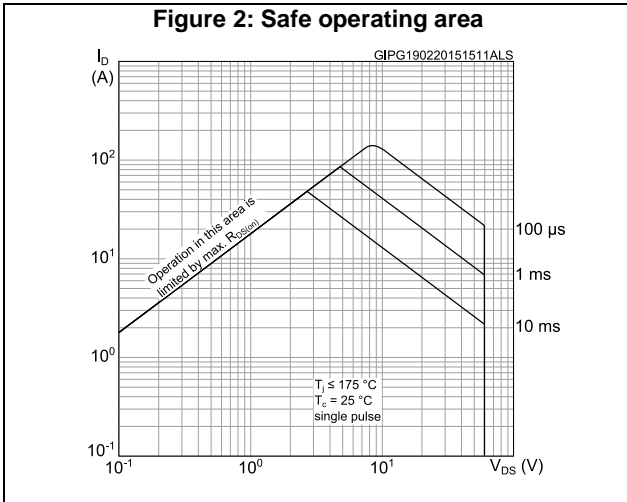
**Notes:**

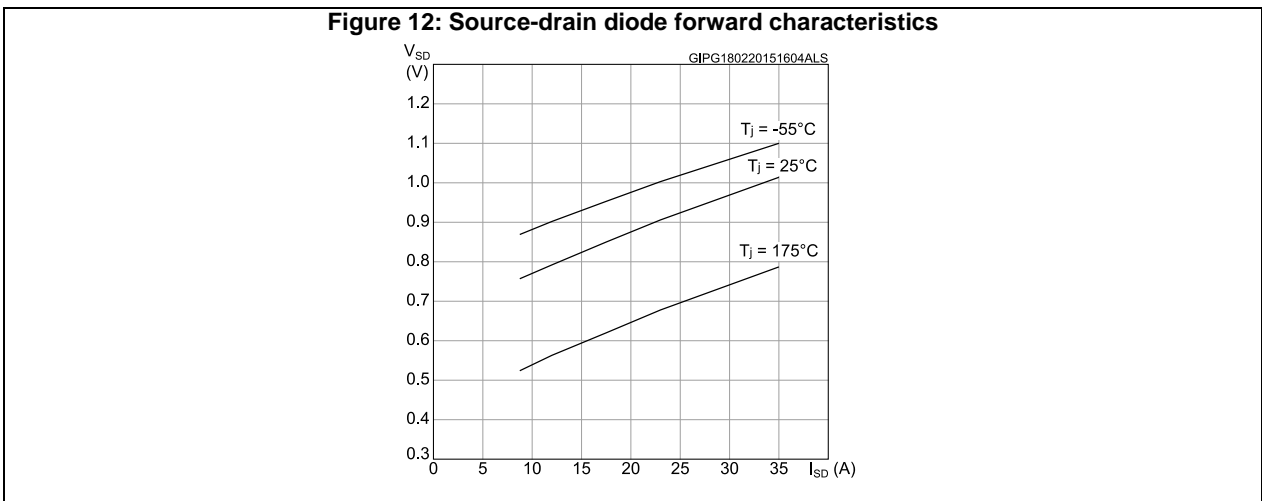
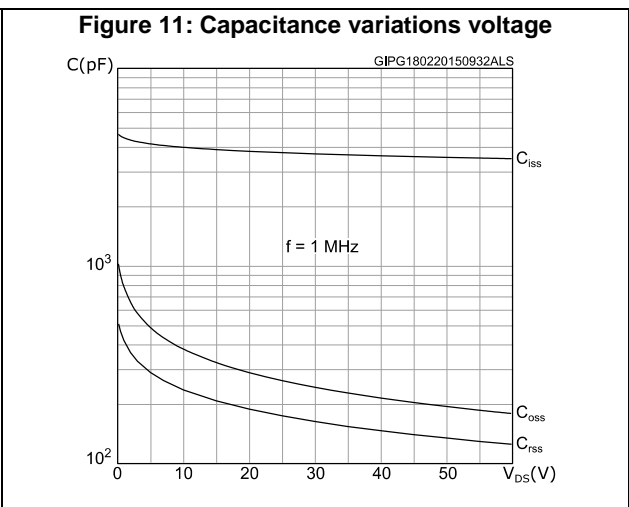
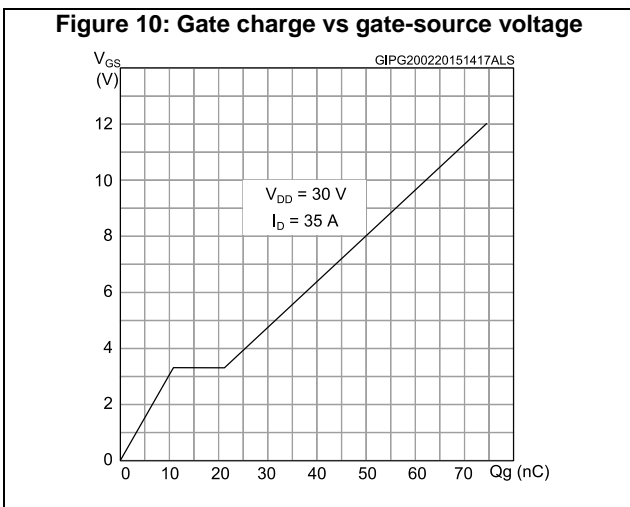
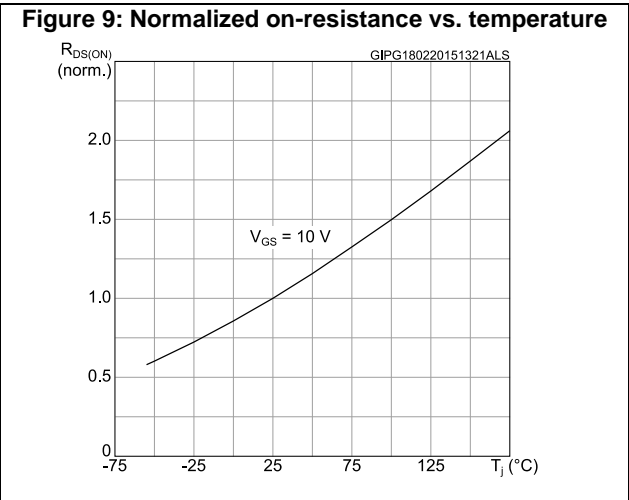
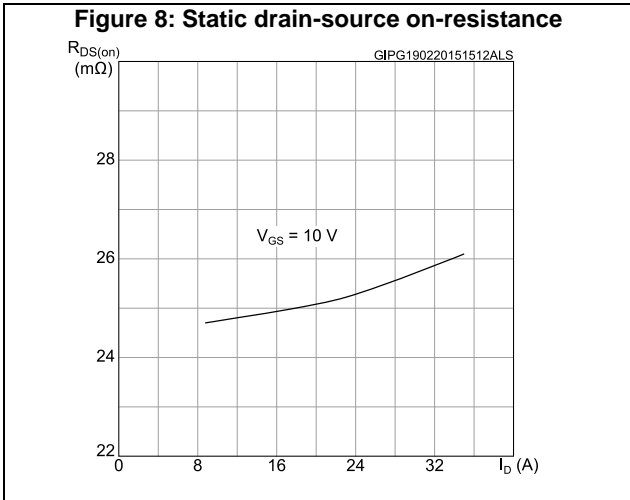
<sup>(1)</sup>Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%



For the P-channel Power MOSFET, current polarity of voltages and current have to be reversed.

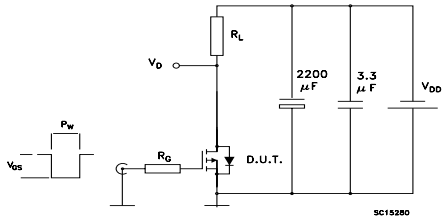
## 2.1 Electrical characteristics (curves)



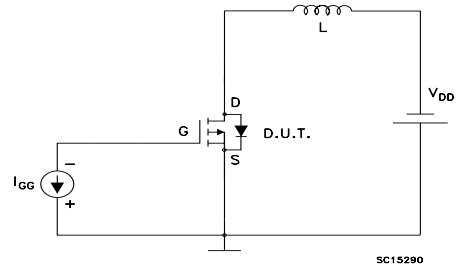


### 3 Test circuits

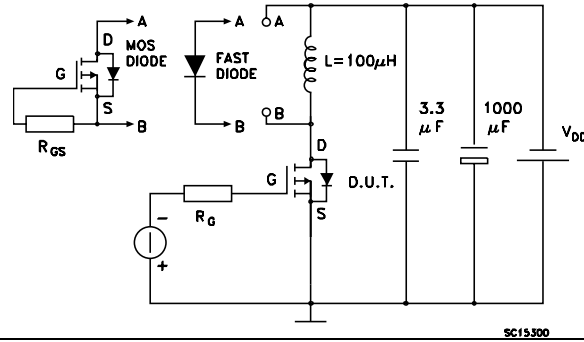
**Figure 13: Switching times test circuit for resistive load**



**Figure 14: Gate charge test circuit**



**Figure 15: Test circuit for inductive load switching and diode recovery times**





## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 DPAK package information

Figure 16: DPAK (TO-252) type A2 package outline

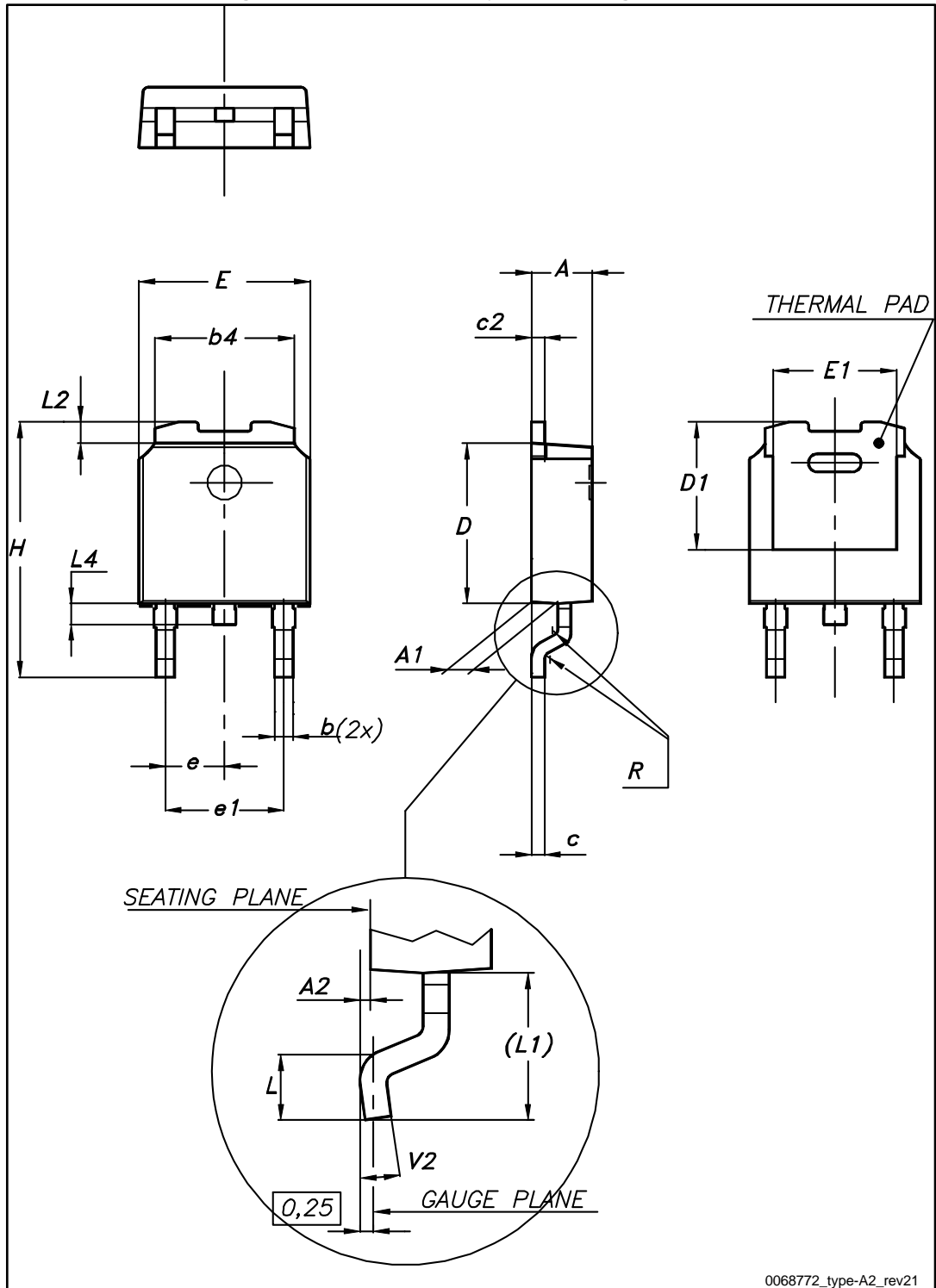
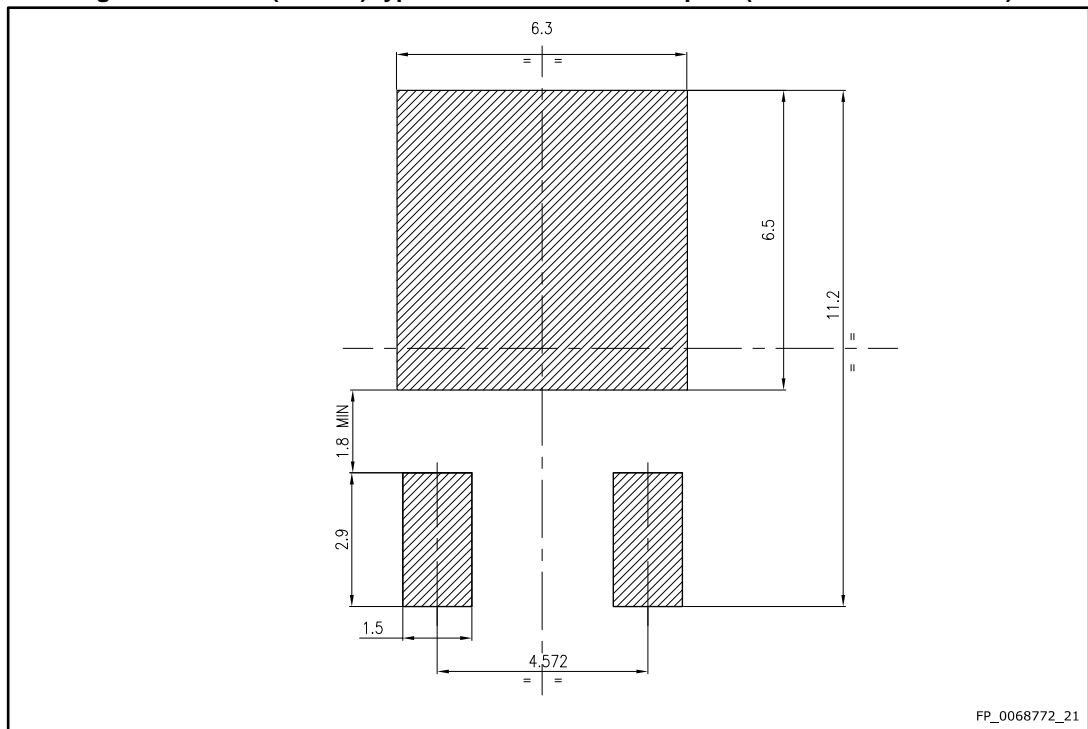


Table 8: DPAK (TO-252) type A2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.16	2.28	2.40
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 17: DPAK (TO-252) type A2 recommended footprint (dimensions are in mm)



### 4.2 Packing information

Figure 18: DPAK (TO-252) tape outline

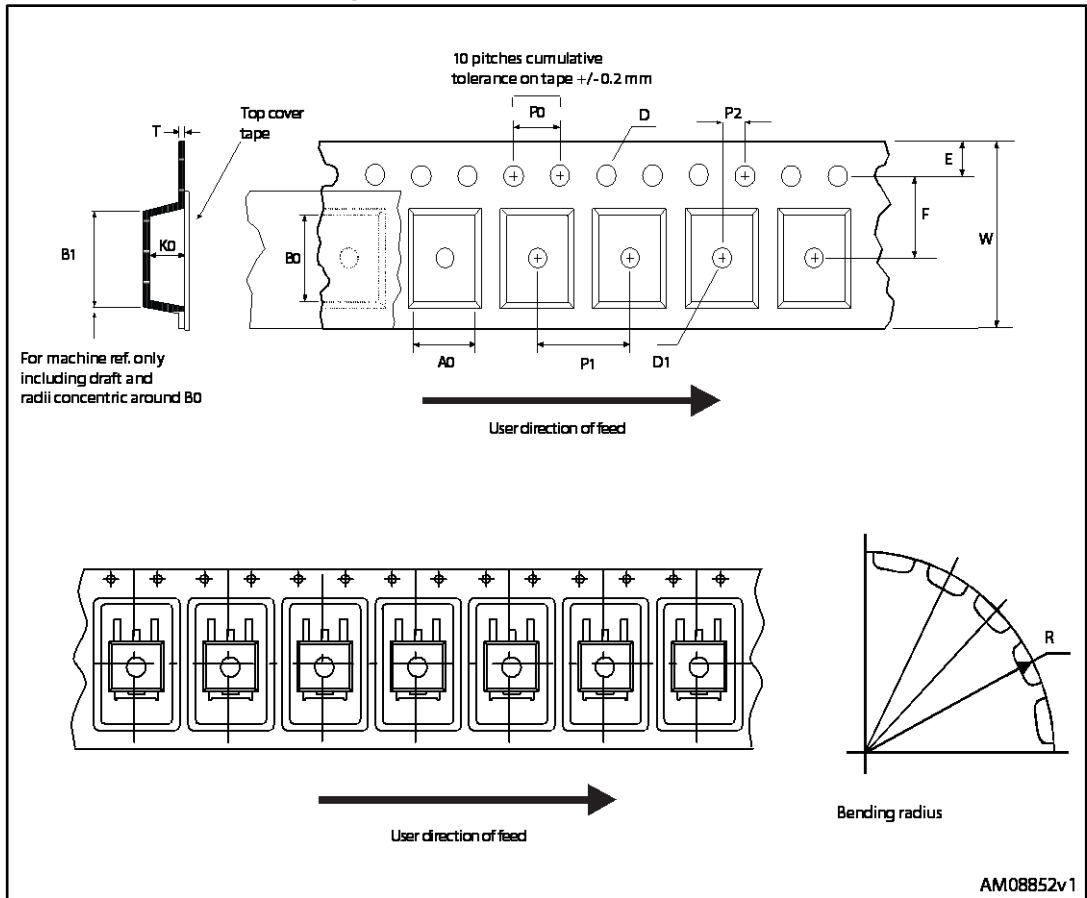
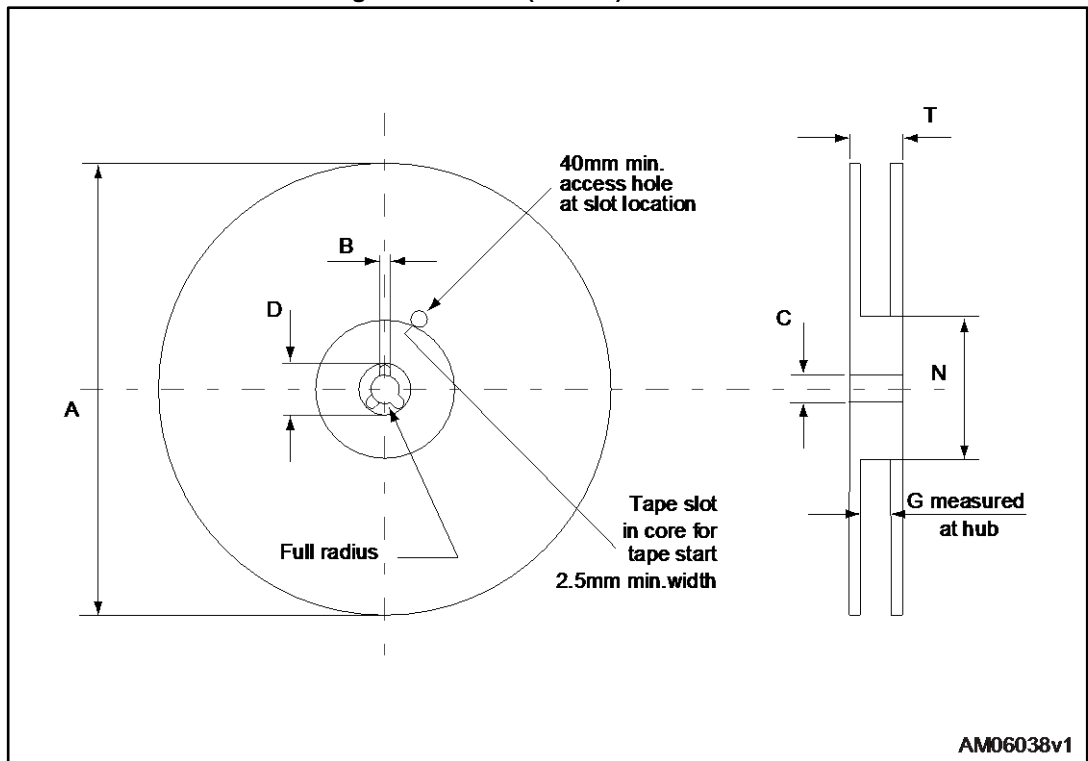


Figure 19: DPAK (TO-252) reel outline



AM06038v1

Table 9: DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

## 5 Revision history

**Table 10: Document revision history**

Date	Revision	Changes
11-Dec-2013	1	First release.
24-Feb-2015	2	<p>In title description on cover page, changed 0.02 <math>\Omega</math> to 0.023 <math>\Omega</math></p> <p>In features table on cover page, changed 0.028 <math>\Omega</math> to 0.026 <math>\Omega</math></p> <p>Updated Table 2: Absolute maximum ratings</p> <p>Updated Table 4: Static – renamed table and updated Static drainsource on-resistance values</p> <p>Updated Table 5: Dynamic – test conditions and all typical values</p> <p>Updated Table 6: Switching times – test conditions and all typical values</p> <p>Updated Table 7: Source-drain diode – test conditions and all typical values</p> <p>Added Section 2.2: Electrical characteristics (curves)</p> <p>Updated Section 4: Package mechanical data Minor text changes</p>
03-Apr-2017	3	<p>Updated <math>V_{SD}</math> maximum value in <a href="#">Table 7: "Source drain diode"</a>.</p> <p>Updated <a href="#">Section 4.1: "DPAK package information"</a></p> <p>Minor text changes.</p>

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