µA555 SINGLE TIMING CIRCUIT FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The μ A555 Timing Circuit is a very stable controller for producing accurate time delays or oscillations. In the time delay mode, the delay time is precisely controlled by one external resistor and one capacitor; in the oscillator mode, the frequency and duty cycle are both accurately controlled with two external resistors and one capacitor. By applying a trigger signal, the timing cycle is started and an internal flip-flop is set, immunizing the circuit from any further trigger signals. To interrupt the timing cycle a reset signal is applied ending the time-out.

The output, which is capable of sinking or sourcing 200 mA, is compatible with TTL circuits and can drive relays or indicator lamps.



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CONNECTION DIAGRAMS

8-PIN MINI DIP

(TOP VIEW) PACKAGE OUTLINE 9T

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CHARACTERISTICS	TEST CONDITIONS	μA555HM			μ A555TC/HC			1
		MIN	ТҮР	MAX	MIN	ТҮР	MAX	UNITS
Supply Voltage		4.5		18	4.5		16	V
Supply Current	$V_{CC} = 5.0 V, R_{L} = \infty$ $V_{CC} = 15 V, R_{L} = \infty$		3.0	5.0		3.0	6.0	mA
	LOW State (Note 1)		10	12		10	15	mA
Timing Error								
Initial Accuracy	R_A , R_B = 1 kΩ to 100 kΩ C = 0.1 μF (Note 2)		0.5	2.0		1.0		%
Drift with Temperature			30	100		50		ppm/
Drift with Supply Voltage			0.05	0.2		0.1		% V
Threshold Voltage			2/3			2/3		X V
Trigger Voltage	V _{CC} = 15 V	4.8	5.0	5.2		5.0		V
	V _{CC} = 5.0 V	1.45	1.67	1.9		1.67		V
Trigger Current			0.5			0.5		μA
Reset Voltage		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current			0.1			0.1		m
Threshold Current	Note 3		0.1	0.25		0.1	0.25	μΑ
Control Voltage Level	V _{CC} = 15 V	9.6	10	10.4	9.0	10	11	V
	V _{CC} = 5.0 V	2.9	3.33	3.8	2.6	3.33	4.0	V
Output Voltage Drop (LOW)	V _{CC} = 15 V							
	ISINK = 10 mA		0.1	0.15		0.1	0.25	V
	ISINK = 50 mA		0.4	0.5		0.4	0.75	V
	ISINK = 100 mA		2.0	2.2		2.0	2.5	V
	I _{SINK} = 200 mA		2.5			2.5		v
	V _{CC} = 5.0 V							
	ISINK = 8.0 mA		0.1	0.25		l l		V
	ISINK = 5.0 mA					0.25	0.35	v
Output Voltage Drop (HIGH)	ISOURCE = 200 mA							
	V _{CC} = 15 V		12.5	1		12.5	1	v
	ISOURCE = 100 mA							
	V _{CC} = 15 V	13	13.3		12.75	13.3		v
	V _{CC} = 5.0 V	3.0	3.3		2.75	3.3		V
Rise Time of Output			100			100		n
Fall Time of Output		1	100			100		n

NOTES:

1. Supply Current is typically 1.0 mA less when output is HIGH. 2. Tested at $V_{CC} = 5.0$ V and $V_{CC} = 15$ V. 3. This will determine the maximum value of $R_A + R_B$. For 15 V operation, the max total R = 20 M Ω . 4. For operating at elevated temperatures the device must be derated based on a +125°C maximum junction temperature and a thermal resistance of +45°C/W junction to case for TO-5 and +150°C/W junction to ambient for both packages.

TYPICAL PERFORMANCE CURVES







LOW OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT SINK CURRENT



LOW OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT SINK CURRENT



LOW OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT SINK CURRENT









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TYPICAL APPLICATIONS

MONOSTABLE OPERATION

In the monostable mode, the timer functions as a one-shot. Referring to Figure 1 the external capacitor is initially held discharged by a transistor inside the timer.

When a negative trigger pulse is applied to lead 2, the flip-flop is set, releasing the short circuit across the external capacitor and drives the output HIGH.The voltage across the capacitor, increases exponentially with the time constant τ = R1C1. When the voltage across the capacitor equals 2/3 V_{CC} , the comparator resets the flip-flop which then discharges the capacitor rapidly and drives the output to its LOW state. Figure 2 shows the actual waveforms generated in this mode of operation.

The circuit triggers on a negative-going input signal when the level reaches $1/3 V_{CC}$. Once triggered, the circuit remains in this state

until the set time has elapsed, even if it is triggered again during this interval. The duration of the output HIGH state is given by t = 1.1 R1C1 and is easily determined by Figure 3. Notice that since the charge rate and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply. Applying a negative pulse simultaneously to the timing cycle discharges the external capacitor and causes the cycle to start over. The timing cycle now starts on the positive edge of the reset pulse. During the time the reset pulse is applied, the output is driven to its LOW state.

When Reset is not used, it should be tied high to avoid any possibility of false triggering.





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TYPICAL APPLICATIONS (Cont'd)

ASTABLE OPERATION

When the circuit is connected as shown in Figure 4 (leads 2 and 6 connected) it triggers itself and free runs as a multivibrator. The external capacitor charges through R1 and R2 and discharges through R2 only. Thus the duty cycle may be precisely set by the ratio of these two resistors.

In the astable mode of operation, C1 charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times and therefore frequency are independent of the supply voltace.

Figure 5 shows actual waveforms generated in this mode of operation.

The charge time (output HIGH) is given by:

t1 = 0.693 (R1 + R2) C1

and the discharge time (output LOW) by:

Thus the total period T is given by:

$$T = t_1 + t_2 = 0.693 (R1 + 2R2) C1$$

The frequency of oscillation is then:

$$f = \frac{1}{T} = \frac{1.44}{(R1 + 2R2) C1}$$

and may be easily found by Figure 6.

The duty cycle is given by:

$$\mathsf{D} = \frac{\mathsf{R}2}{\mathsf{R}1 + 2\mathsf{R}2}$$









Fig. 6

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